

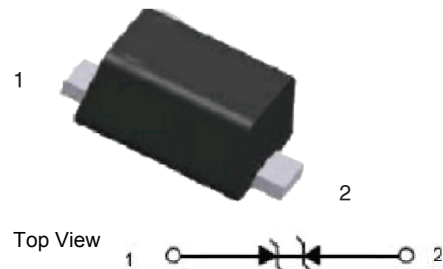
TVS Diodes

1KE1G3V0C ~ 1KE1G5V0C

■ Features

- Low Clamping Voltage.
- Small Body Outline Dimensions..
- Low Leakage
- ESD Rating of Class 3(>16kV) per Human Body
- IEC61000-4-2 Level 4 ESD Protection IEC61000-4-4 Level 4 EFT Protection

SOD-523



PIN DESCRIPTION

PIN	DESCRIPTION
1	Cathode
2	Anode

■ Absolute Maximum Ratings Ta = 25°C

Parameter	Symbol	Value	Unit
IEC 61000-4-2(ESD) Contact Air		±30	KV
		±30	
IEC 61000-4-4(EFT)		40	A
ESD Voltage Per Human Body Model		16	KV
Total Power Dissipation on FR-4 Board *1	P _D	500	mW
Junction Temperature	T _J	150	°C
Storage Temperature range	T _{stg}	-55 to +150	
Lead Solder Temperature - Maximum (10 Second Duration)	TL	260	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

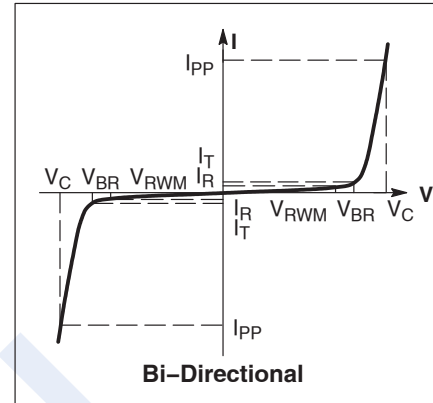
*1. FR-4 printed circuit board, single-sided copper, mounting pad 1 cm²

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■ Electrical Characteristics Ta = 25°C unless otherwise noted

Symbol	Parameter
I _{PP}	Maximum Reverse Peak Pulse Current
V _C	Clamping Voltage @ I _{PP}
V _{RWM}	Working Peak Reverse Voltage
I _R	Maximum Reverse Leakage Current @ V _{RWM}
V _{BR}	Breakdown Voltage @ I _T
I _T	Test Current
C	Capacitance @ V _R = 0 V and f = 1.0 MHz



■ Electrical Characteristics Ta = 25°C

Device**	Device Marking	V _{RWM} (V)	I _R (nA) @ V _{RWM}	V _{BR} (V) @ I _T (Note 2)	I _T	V _C (V) @ I _{PP} = 5.0 A†	V _C (V) @ Max I _{PP} †	I _{PP} (A)†	P _{pk} (W)†	C (pF)
		Max	Max	Min	mA	Typ	Max	Max	Max	Typ
1KE1G3V0C	3C	3.0	100	4.0	1.0	7.5	12.9	11.0	137	125
1KE1G3V3C	3D	3.3	100	5.0	1.0	8.4	14.1	11.2	158	105
1KE1G5V0C	5C	5.0	100	5.6	1.0	11.6	18.6	9.4	174	80

**Other voltages available upon request.

1. Surge current waveform per Figure 5.
2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25 °C
3. For test procedure see Figures 3 and 4.

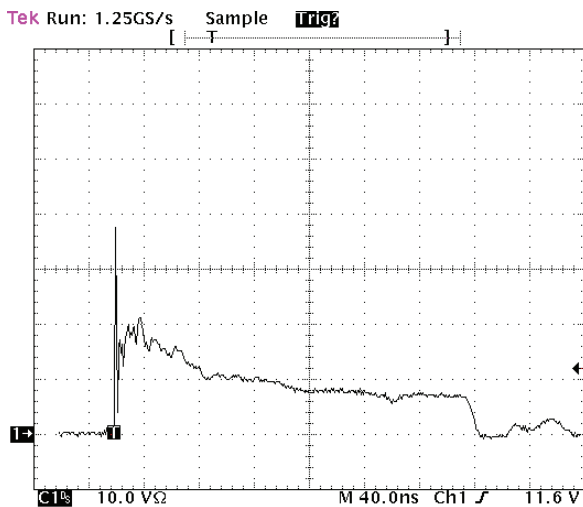


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV contact per IEC 61000-4-2

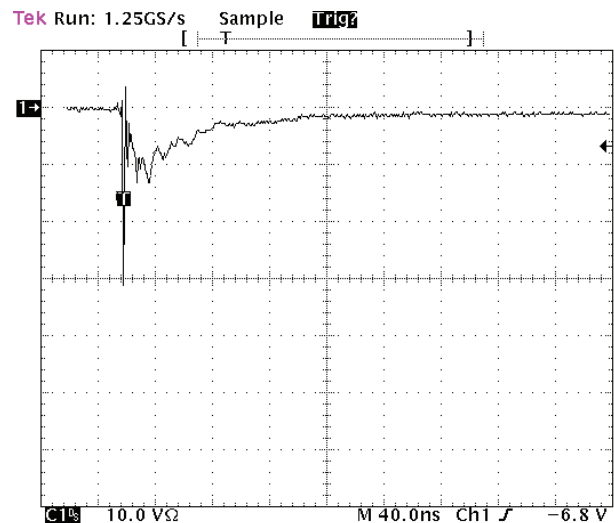


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV contact per IEC 61000-4-2

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IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

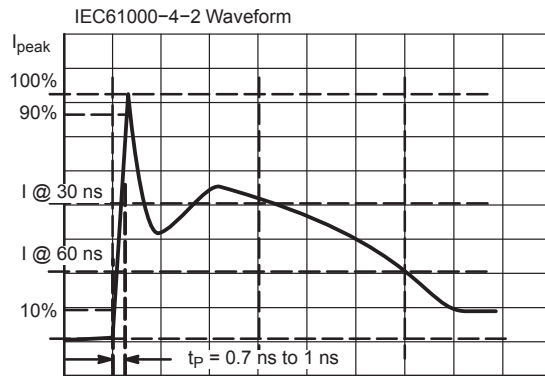


Figure 3. IEC61000-4-2 Spec

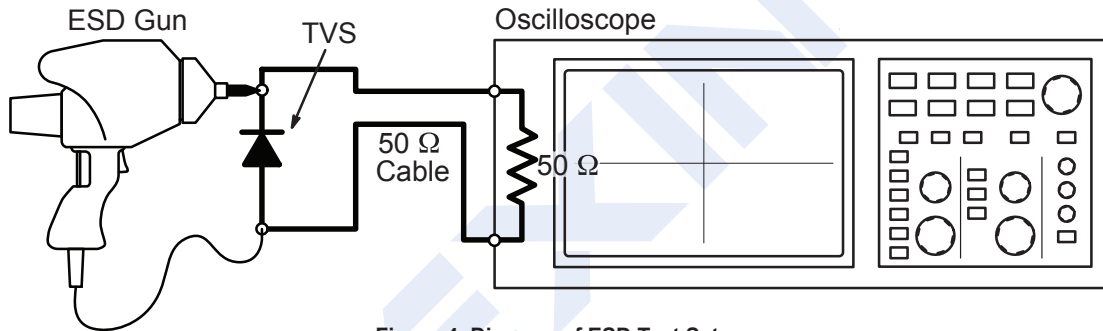


Figure 4. Diagram of ESD Test Setup

ESD Voltage Clamping

For sensitive circuit elements, it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level.

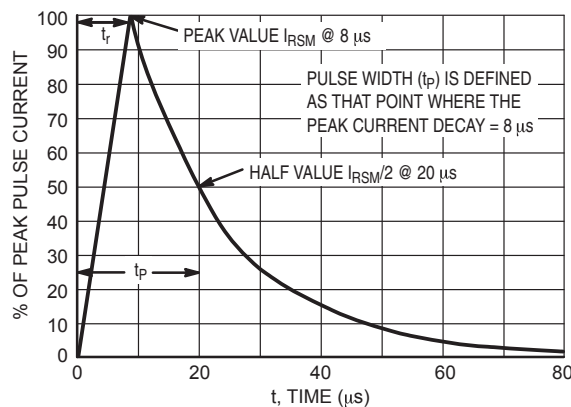
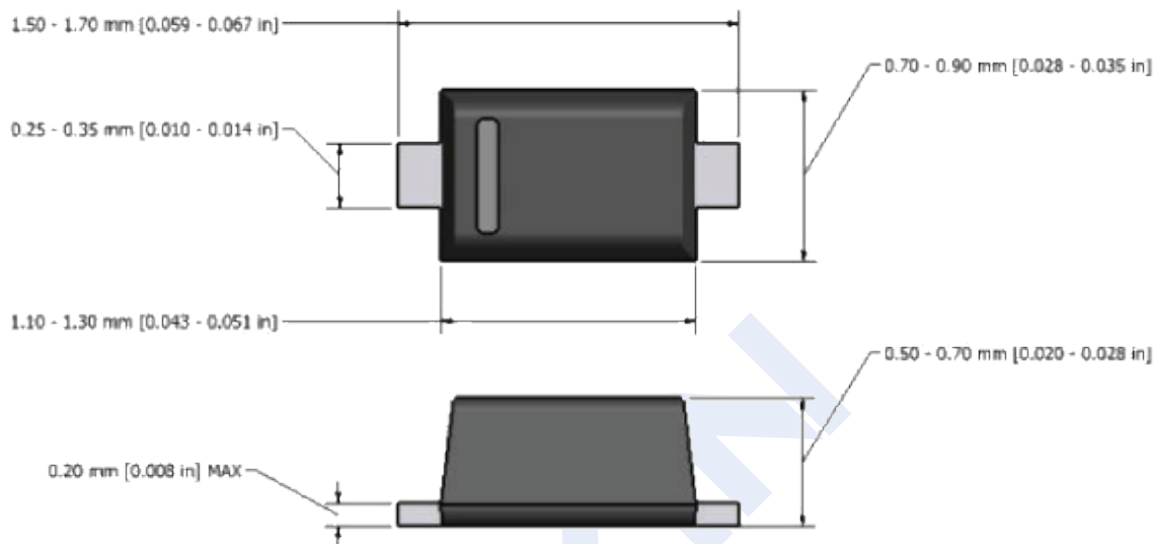


Figure 5. 8 X 20 μs Pulse Waveform

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■ Package Outline Dimensions (SOD-523)



Note: Dimensions are exclusive of Burrs, Mold Flash & Tie Bar extrusions.

■ The Recommended Mounting Pad Size

