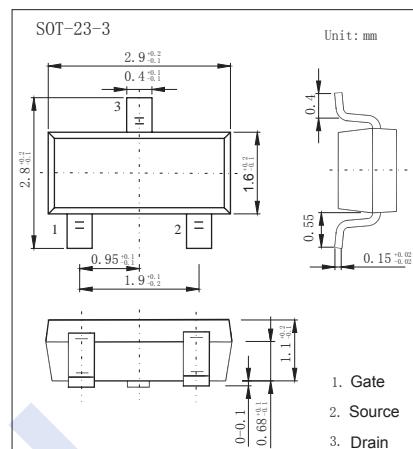


P-Channel Enhancement MOSFET

2KJ6007

■ Features

- VDS (V) = -20V
- Low ON-resistance:
 - $R_{DS(ON)} = 88.4\text{m}\Omega$ (VGS = -1.5V)
 - $R_{DS(ON)} = 56\text{m}\Omega$ (VGS = -1.8V)
 - $R_{DS(ON)} = 39.7\text{m}\Omega$ (VGS = -2.5V)
 - $R_{DS(ON)} = 29.8\text{m}\Omega$ VGS = -4.5 V



■ Absolute Maximum Ratings Ta = 25°C

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V _{DS}	-20	V
Gate-Source Voltage	V _{Gs}	±8	
Continuous Drain Current *1	I _D	-6.0	A
Pulsed Drain Current *2	I _{DM}	-24	
Power Dissipation *3	P _D	1	W
Power Dissipation t=10s		2	
Junction Temperature	T _J	150	°C
Junction and Storage Temperature Range	T _{stg}	-55 to 150	

*1 The channel temperature should not exceed 150°C during use.

*2 PW ≤ 10μs, Duty ≤ 1%

*3 Mounted on a FR4 board.

P-Channel Enhancement MOSFET

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■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V _{DSS}	I _D = -1mA, V _{GS} =0V	-20			V
	V _{DS}	I _D = -1mA, V _{GS} =5V *1	-15			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	μA
Gate-Body leakage current	I _{GSS}	V _{DS} = ± 8V, V _{GS} =0V			±1	μA
Gate Threshold Voltage	V _{GS(off)}	V _{DS} =-3V I _D =-1mA	-0.3		-1.0	V
Forward transfer admittance	g _{fs}	V _{DS} = -3 V, I _D = -1.0 A *2	4.5	9.1		S
Static Drain-Source On-Resistance	R _{D(on)}	V _{GS} =-4.5V, I _D =-3.0A *2		24.9	29.8	mΩ
		V _{GS} =-2.5V, I _D =-2.5A *2		31.1	39.7	
		V _{GS} =-1.8V, I _D =-1.5A *2		38.8	56	
		V _{GS} =-1.5V, I _D =-0.5A *2		47.4	88.4	
Input Capacitance	C _{iss}	V _{GS} =0V, V _{DS} =-10V, f=1MHz		840		pF
Output Capacitance	C _{oss}			118		
Reverse Transfer Capacitance	C _{rss}			99		
Total Gate Charge	Q _g	V _{GS} =-4.5V, V _{DD} =-10V, I _{DS} =-4A		12.8		nC
Gate Source Charge	Q _{gs}			1.4		
Gate Drain Charge	Q _{gd}			3.0		
Turn-On DelayTime	t _{d(on)}	V _{GS} =0 to -25V, V _{DD} =-10V, I _D =-2.0A, R _{GEN} =4.7Ω		32		ns
Turn-Off DelayTime	t _{d(off)}			107		
Diode Forward Voltage	V _{SD}	I _D =6.0 A, V _{GS} =0V		0.87	1.2	V

*1 VDSX mode (the application of a plus voltage between gate and source) may cause decrease in maximum rating of drain-source voltage

*2 Pulse test

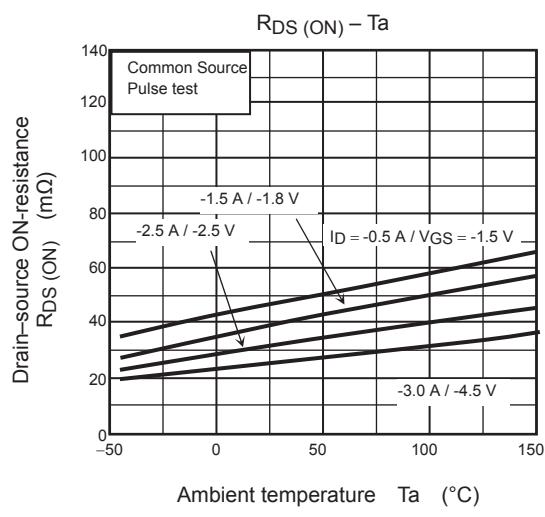
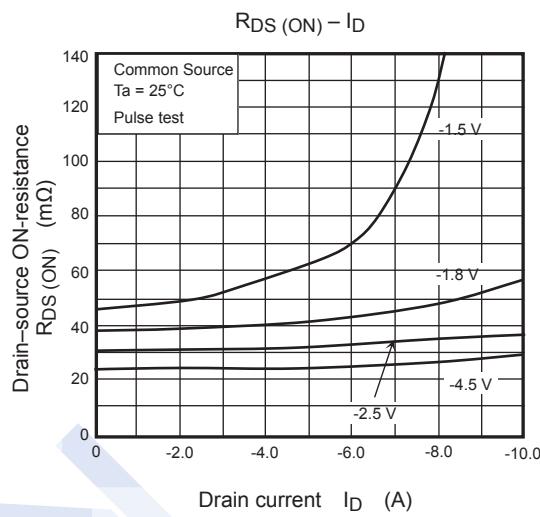
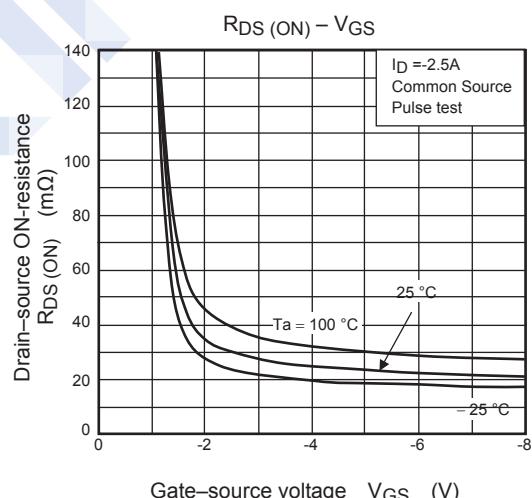
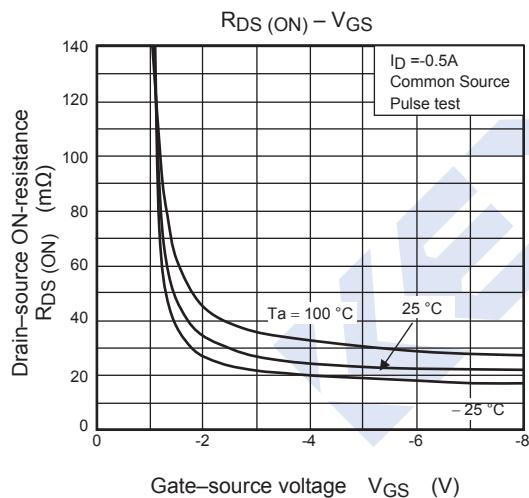
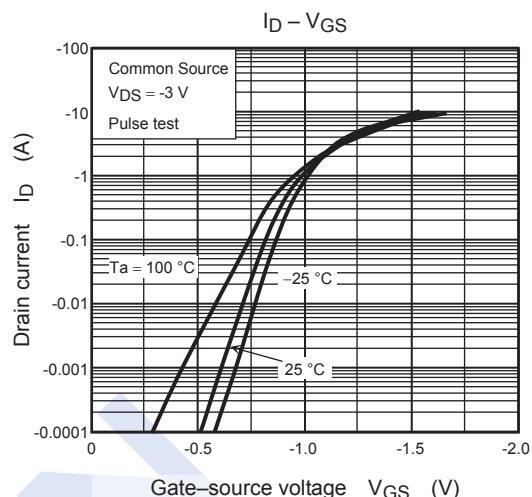
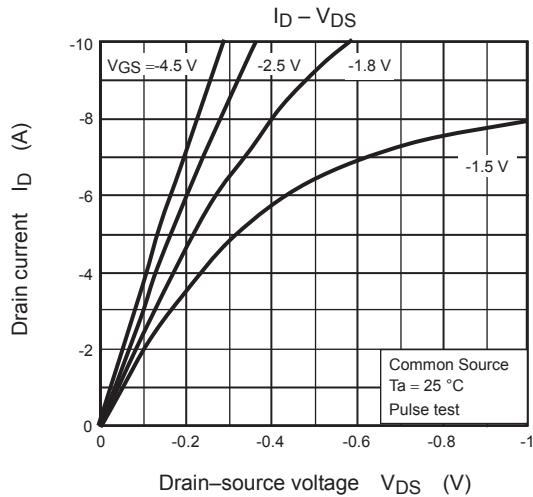
■ Marking

Marking	JA7
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P-Channel Enhancement MOSFET

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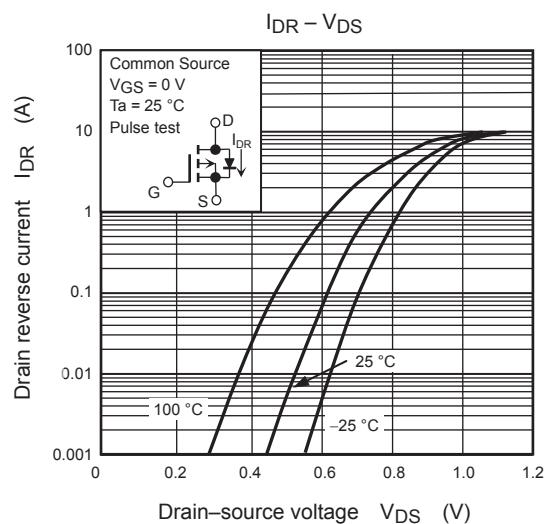
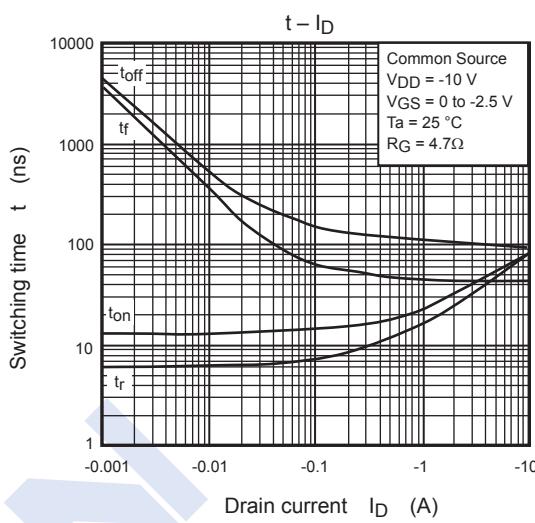
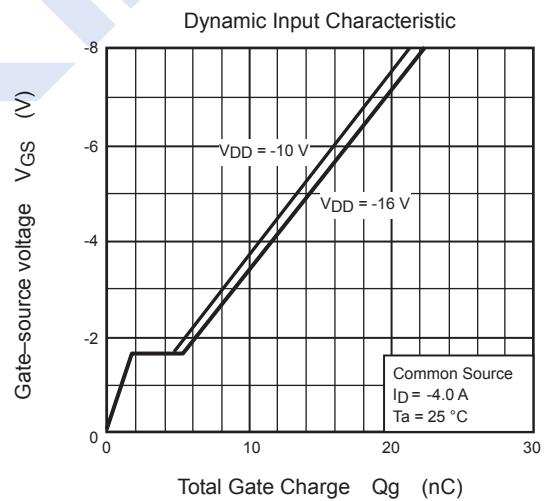
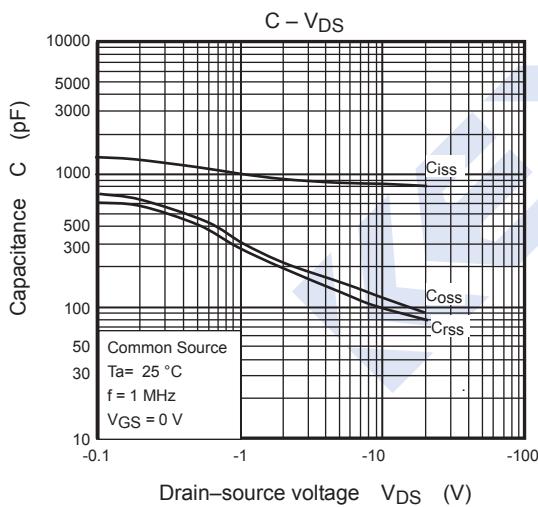
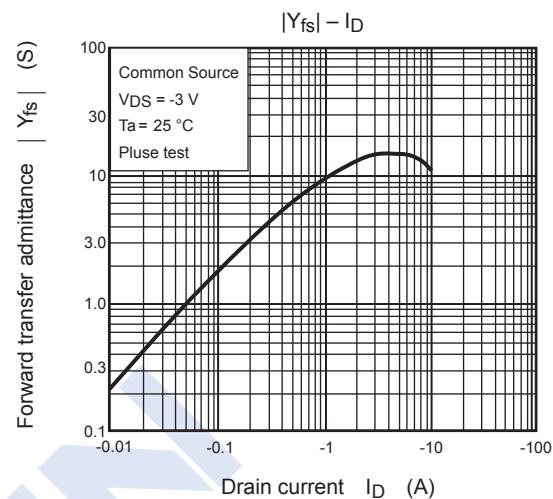
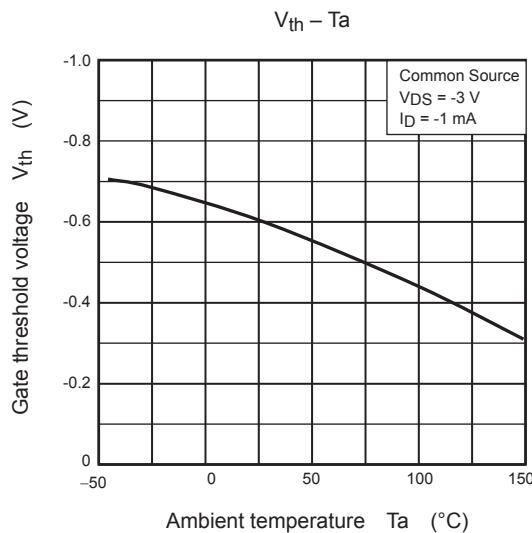
■ Typical Characteristics



P-Channel Enhancement MOSFET

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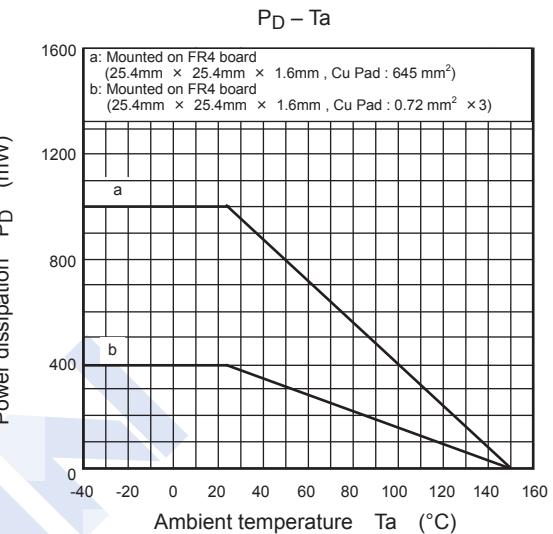
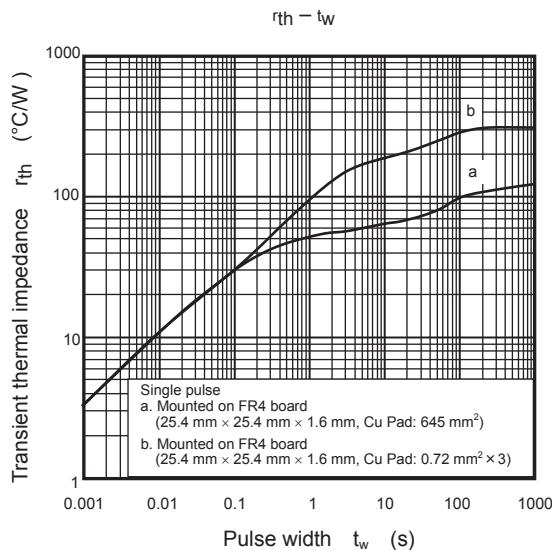
■ Typical Characteristics



P-Channel Enhancement MOSFET

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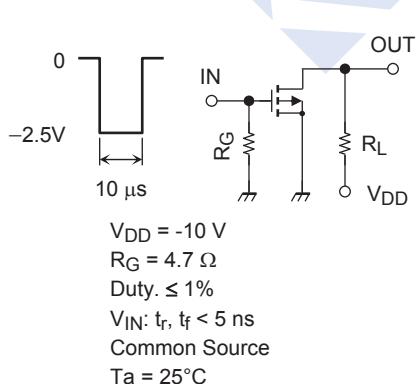
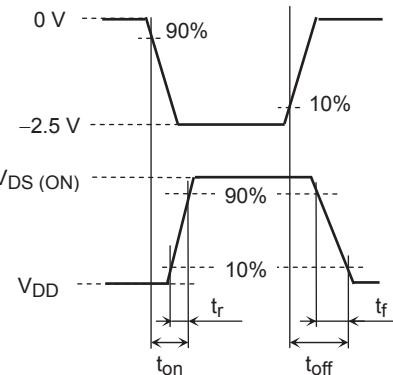
■ Typical Characteristics



■ Typical Application

Switching Time Test Circuit

(a) Test Circuit

(b) V_{IN} (c) V_{OUT} 