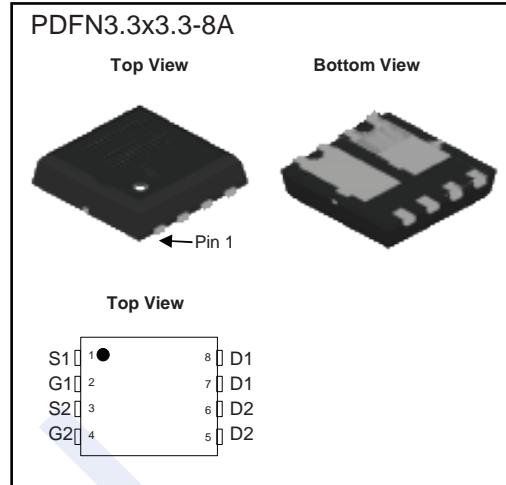
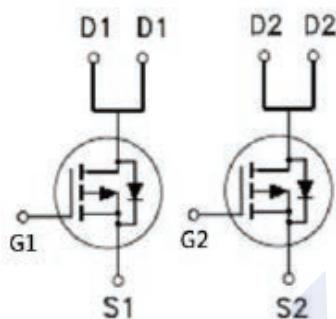


Dual P-Channel MOSFET

2KJ6064DFN

■ Features

- V_{DS} -30 V
- I_D (at $V_{GS}=-10V$) -23 A
- $R_{DS(ON)}$ (at $V_{GS} = - 10V$) < 32 mΩ
- $R_{DS(ON)}$ (at $V_{GS} = - 4.5V$) < 44 mΩ

■ Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted.)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current (Note 1)	I_D	-23	A
		-14	
Pulsed Drain Current (Note 2)	I_{DM}	-50	
Avalanche Current	I_{AR}	24	
Repetitive avalanche energy $L=0.1mH$	E_{AR}	29	mJ
Power Dissipation (Note 1)	P_D	25	W
		10	
		4.1	
Thermal Resistance, Junction- to-Lead (Note 1)	$R_{\theta JC}$	5	°C/W
Thermal Resistance, Junction- to-Ambient (Note 1)	$R_{\theta JA}$	30	
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{Stg}	-55 to 150	

Notes:

1. Surface mounted on 1.5" x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.
2. Pulse width limited by maximum junction temperature.

Dual P-Channel MOSFET

2KJ6064DFN

■ Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$\text{I}_D = -250\mu\text{A}, \text{V}_{\text{GS}} = 0\text{V}$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$\text{V}_{\text{DS}} = -30\text{V}, \text{V}_{\text{GS}} = 0\text{V}$			-1	μA
		$\text{V}_{\text{DS}} = -30\text{V}, \text{V}_{\text{GS}} = 0\text{V}, \text{T}_J = 55^\circ\text{C}$			-5	
Gate-Body Leakage Current	I_{GSS}	$\text{V}_{\text{DS}} = 0\text{V}, \text{V}_{\text{GS}} = \pm 20\text{V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$\text{V}_{\text{GS(th)}}$	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}, \text{I}_D = -250\mu\text{A}$	-1.0		-2.0	V
Static Drain-Source On-Resistance (Note 3)	$\text{R}_{\text{DS(on)}}$	$\text{V}_{\text{GS}} = -10\text{V}, \text{I}_D = -8\text{A}$			32	$\text{m}\Omega$
		$\text{V}_{\text{GS}} = -4.5\text{V}, \text{I}_D = -5\text{A}$			44	
Diode Forward Voltage (Note 3)	V_{SD}	$\text{I}_S = -5\text{ A}, \text{V}_{\text{GS}} = 0\text{V}$			-1.2	V
DYNAMIC CHARACTERISTICS (Note 4)						
Input Capacitance	C_{iss}	$\text{V}_{\text{GS}} = 0\text{V}, \text{V}_{\text{DS}} = -15\text{V}, \text{f} = 1\text{MHz}$		904	1760	pF
Output Capacitance	C_{oss}			192		
Reverse Transfer Capacitance	C_{rss}			124		
Gate resistance	R_{g}	$\text{V}_{\text{GS}} = 0\text{V}, \text{V}_{\text{DS}} = 0\text{V}, \text{f} = 1\text{MHz}$		6		Ω
Total Gate Charge	Q_{g}	$\text{V}_{\text{DS}} = -15\text{V}, \text{V}_{\text{GS}} = -10\text{V}, \text{I}_D = -8\text{A}$		14.4		nC
Gate Source Charge	Q_{gs}			4.4		
Gate Drain Charge	Q_{gd}			2.6		
SWITCHING CHARACTERISTICS (Note 5)						
Turn-On Delay Time	$\text{t}_{\text{d(on)}}$	$\text{V}_{\text{GS}} = -10\text{V}, \text{V}_{\text{DS}} = -15\text{V}, \text{R}_{\text{L}} = 1.8\Omega, \text{R}_{\text{GEN}} = 3\Omega$		9		ns
Turn-On Rise Time	t_{r}			8		
Turn-Off Delay Time	$\text{t}_{\text{d(off)}}$			18		
Turn-Off Fall Time	t_{f}			7		
Reverse Recovery Time	t_{rr}	$\text{I}_{\text{F}} = -8\text{A}, \text{dI}/\text{dt} = 500\text{A}/\mu\text{s}$		12		ns
Reverse Recovery Charge	Q_{rr}			26		μC

Notes:

3. Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
4. For design aid only, not subject to production testing.
5. Switching characteristics are independent of operating junction temperatures.

■ Marking

Marking	J6064 KA****
---------	-----------------

Dual P-Channel MOSFET

2KJ6064DFN

■ Typical Electrical and Thermal Characteristics

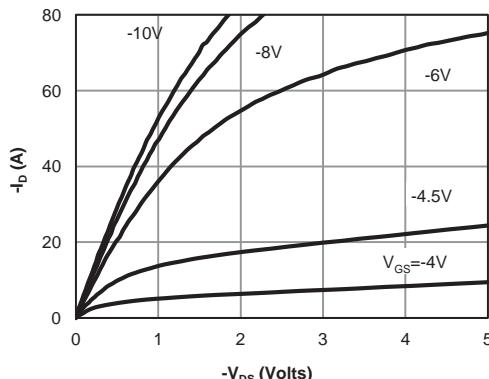


Fig 1: On-Region Characteristics

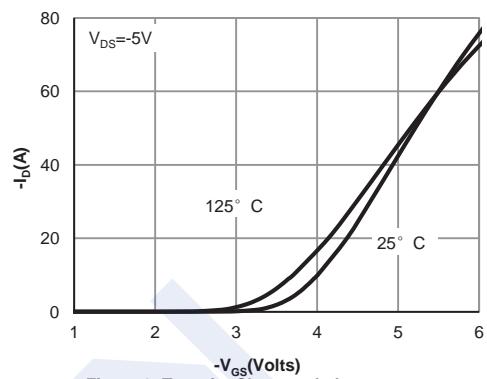


Figure 2: Transfer Characteristics

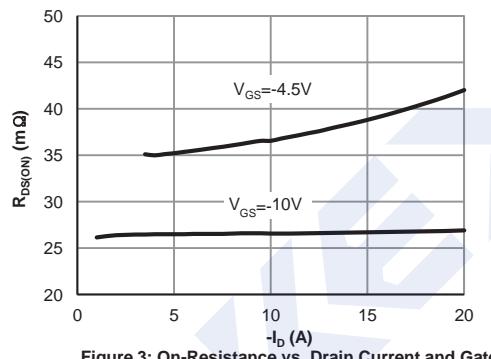


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

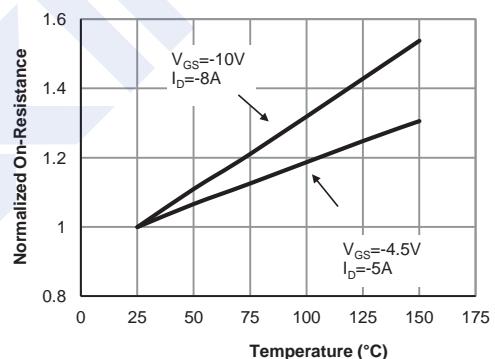


Figure 4: On-Resistance vs. Junction Temperature

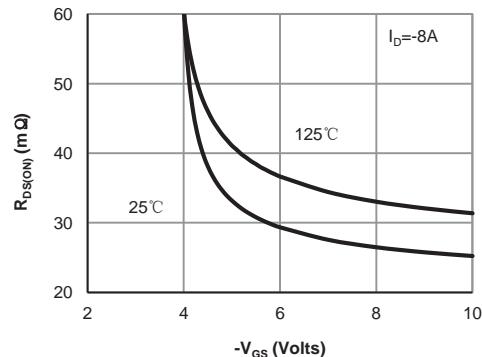


Figure 5: On-Resistance vs. Gate-Source Voltage

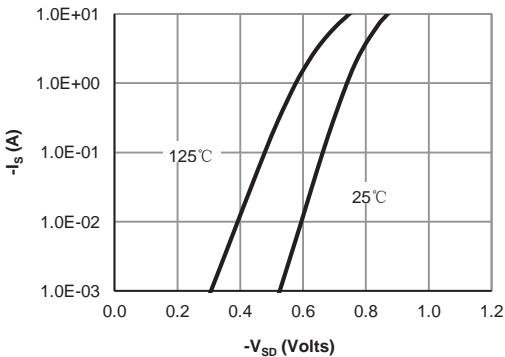


Figure 6: Body-Diode Characteristics

Dual P-Channel MOSFET

2KJ6064DFN

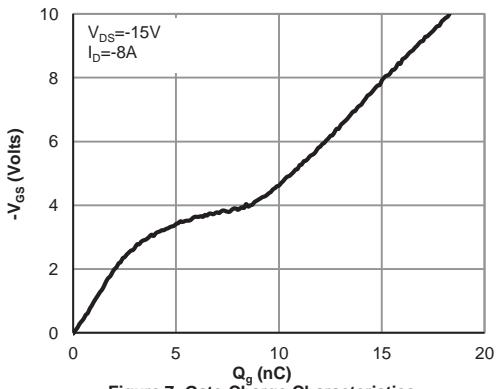


Figure 7: Gate-Charge Characteristics

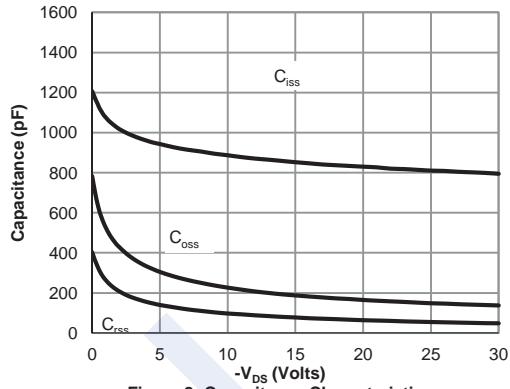


Figure 8: Capacitance Characteristics

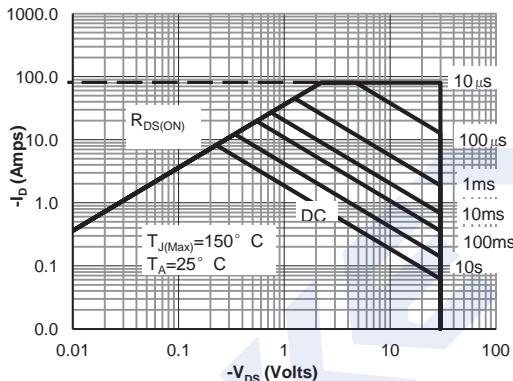


Figure 9: Maximum Forward Biased Safe Operating Area

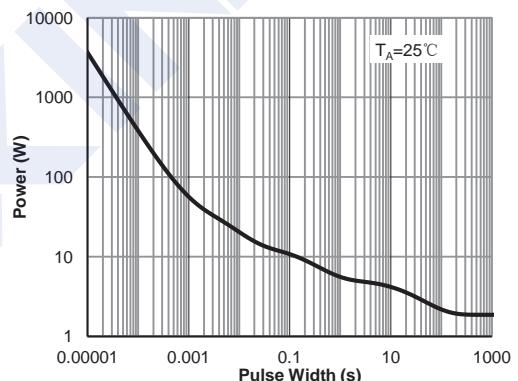


Figure 10: Single Pulse Power Rating Junction-to-Ambient

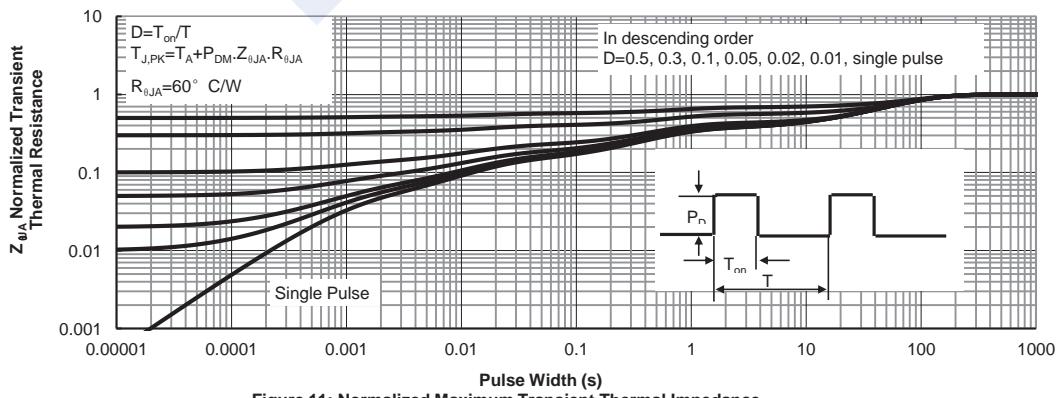


Figure 11: Normalized Maximum Transient Thermal Impedance

Dual P-Channel MOSFET**2KJ6064DFN****■ PDFN3.3x3.3-8A Package Outline Dimensions**