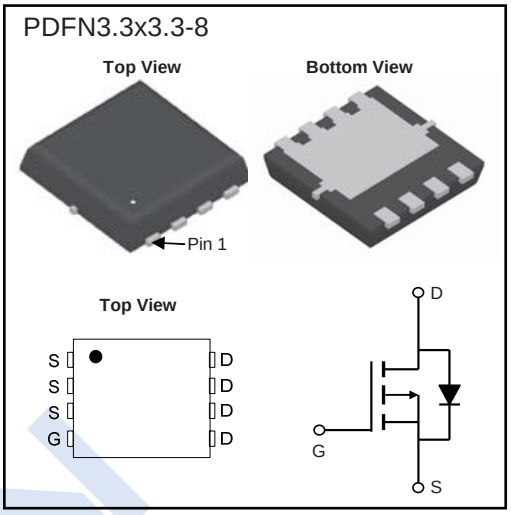
# P-Channel MOSFET

# 2KJ7105DFN

## Features

- $V_{DS}$ -20V
- $I_D$ (at $V_{GS}$=-4.5V) -40A
- $R_{DS(ON)}$ (at $V_{GS}$ =-4.5V) < 9.5mΩ
- $R_{DS(ON)}$ (at $V_{GS}$ =-2.5V) < 12.5mΩ
- $R_{DS(ON)}$ (at $V_{GS}$ =-1.8V) < 18mΩ




## Absolute Maximum Ratings $T_A$ = 25℃ unless otherwise noted.

| Parameter | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±8 | |
| Continuous Drain Current | $T_C$=25℃ | $I_D$ | -40 | A |
| | $T_C$=100℃ | | -29 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | -100 | |
| Continuous Drain Current | $T_A$=25℃ | $I_{DSM}$ | -14.5 | |
| | $T_A$=70℃ | | -11.5 | |
| Avalanche Current [C] | | $I_{AS}$, $I_{AR}$ | -40 | |
| Avalanche energy L=0.1mH [C] | | $E_{AS}$, $E_{AR}$ | 80 | mJ |
| Power Dissipation [B] | $T_C$=25℃ | $P_D$ | 29 | W |
| | $T_C$=100℃ | | 12 | |
| Power Dissipation [A] | $T_A$=25℃ | $P_{DSM}$ | 3.1 | |
| | $T_A$=70℃ | | 2 | |
| Thermal Resistance.Junction- to-Ambient [A] | t ≤ 10s | $R_{thJA}$ | 40 | ℃/W |
| Thermal Resistance.Junction- to-Ambient [A D] | Steady-State | | 75 | |
| Thermal Resistance.Junction- to-Case | Steady-State | $R_{thJC}$ | 4.2 | |
| Junction Temperature | | $T_J$ | 150 | ℃ |
| Storage Temperature Range | | $T_{stg}$ | -55 to 150 | |

A. The value of $R_{JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25°C. The Power dissipation $P_{DSM}$ is based on $R_{\theta JA}$ t ≤ 10s value and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial $T_J$=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

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## ■ Electrical Characteristics ($T_J$ = 25℃ unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = -250μA, $V_{GS}$ = 0V | -20 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$= -20V, $V_{GS}$ = 0V | | | -1 | μA |
| | | $V_{DS}$= -20V, $V_{GS}$ = 0V, $T_J$ = 25℃ | | | -5 | |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0V, $V_{GS}$ = ±8V | | | ±100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$ , $I_D$ = -250μA | -0.3 | | -0.9 | V |
| On state drain current | $I_{D(ON)}$ | $V_{GS}$=-4.5V, $V_{DS}$=-5V | -100 | | | A |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}$ = -4.5V, $I_D$ = -14A | | | 9.5 | mΩ |
| | | $V_{GS}$ = -4.5V, $I_D$ = -14A, $T_J$ = 125℃ | | | 13.5 | |
| | | $V_{GS}$ = -2.5V, $I_D$ = -13A | | | 12.5 | |
| | | $V_{GS}$ = -1.8V, $I_D$ = -11A | | | 18 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = -5V, $I_D$ = -14A | | 72 | | S |
| Input Capacitance | $C_{iss}$ | $V_{GS}$=0V, $V_{DS}$ = -10V, f = 1MHz | 2795 | 3495 | 4195 | pF |
| Output Capacitance | $C_{oss}$ | | 365 | 528 | 690 | |
| Reverse Transfer Capacitance | $C_{rss}$ | | 255 | 425 | 595 | |
| Gate resistance | Rg | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | | | 5.6 | Ω |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = -10V, $I_D$ = -14A $V_{GS}$ = -4.5V | 35 | 44 | 53 | nC |
| Gate Source Charge | $Q_{gs}$ | | | 9 | | |
| Gate Drain Charge | $Q_{gd}$ | | | 11 | | |
| Turn-On DelayTime | $t_{d(on)}$ | $V_{GS}$ = -4.5V, $V_{DS}$ = -10V, $R_L$ = 0.75Ω, $R_{GEN}$ = 3Ω | | 18 | | ns |
| Turn-On Rise Time | $t_r$ | | | 32 | | |
| Turn-Off DelayTime | $t_{d(off)}$ | | | 136 | | |
| Turn-Off Fall Time | $t_f$ | | | 59 | | |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $I_F$= -14A, $dI/dt$= 500A/μs | 26 | 33 | 40 | |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | $I_F$= -14A, $dI/dt$= 500A/μs | 80 | 100 | 120 | nC |
| Maximum Body-Diode Continuous Current | $I_S$ | | | | -35 | A |
| Diode Forward Voltage | $V_{SD}$ | $I_S$ = -1 A,$V_{GS}$ = 0V | | | -1 | V |

E. The static characteristics in Figures 1 to 6 are obtained using <300s pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 $in^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25°C.

## ■ Marking

| | |
|---|---|
| Marking | J7105<br>KC*** |

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■ Typical Electrical and Thermal Characterisitics

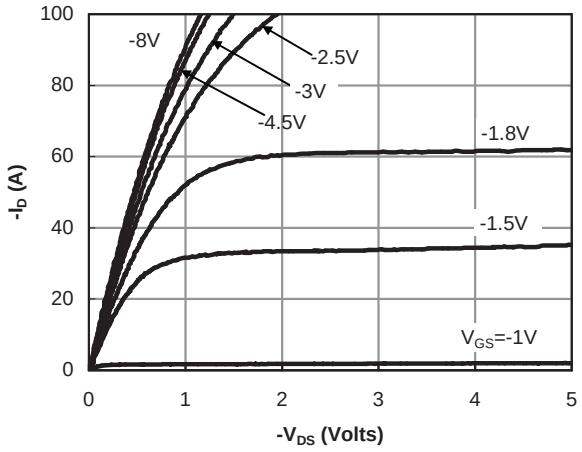


Fig 1: On-Region Characteristics (Note E)

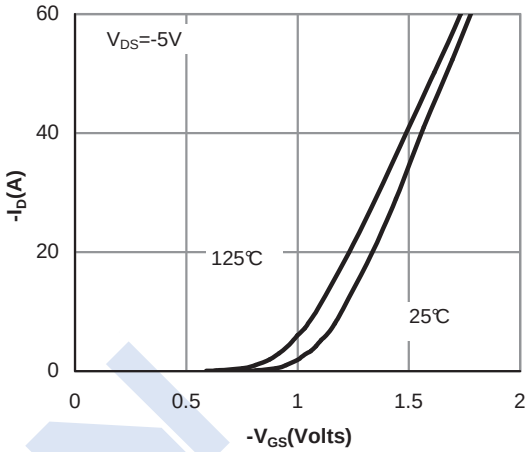


Figure 2: Transfer Characteristics (Note E)

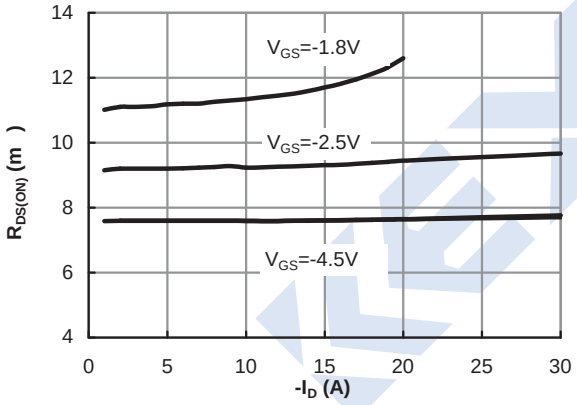


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

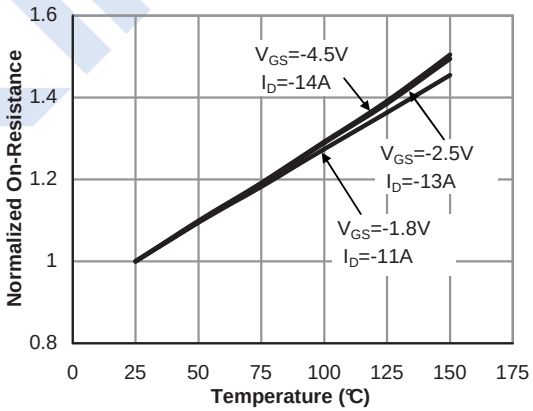


Figure 4: On-Resistance vs. Junction Temperature (Note E)

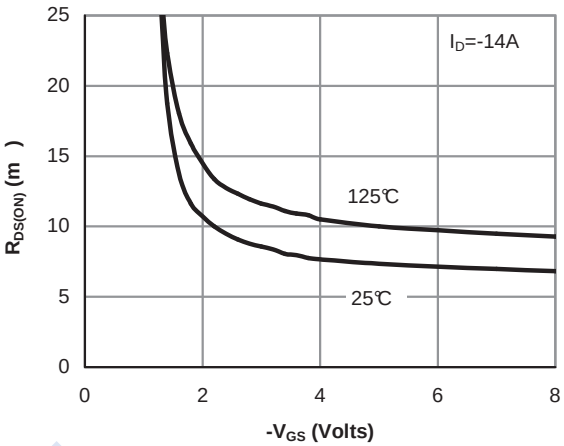


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

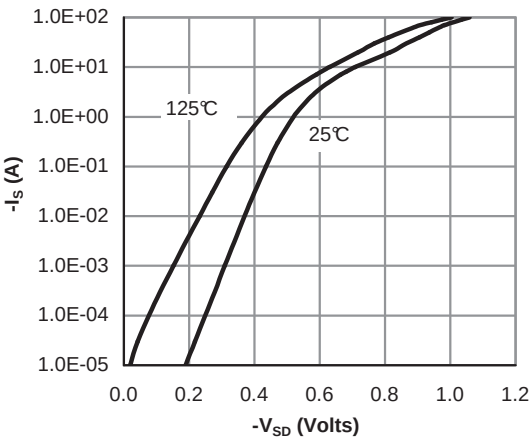


Figure 6: Body-Diode Characteristics (Note E)

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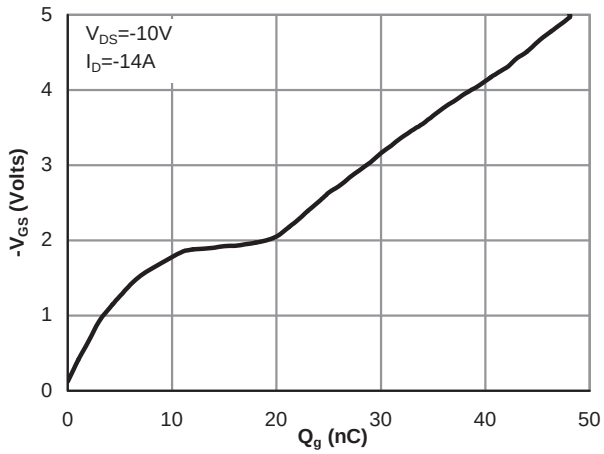


Figure 7: Gate-Charge Characteristics

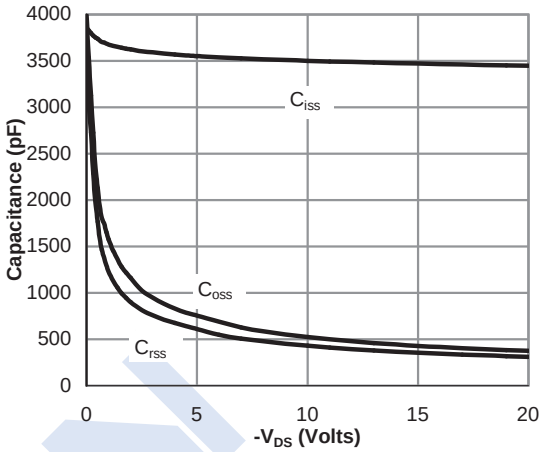


Figure 8: Capacitance Characteristics

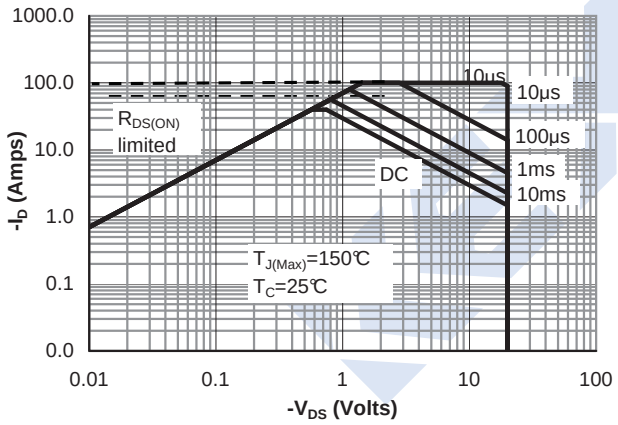


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

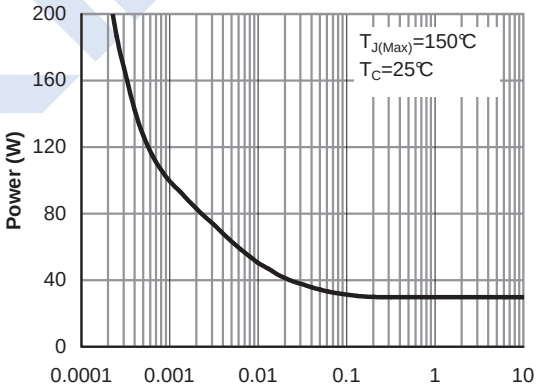


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

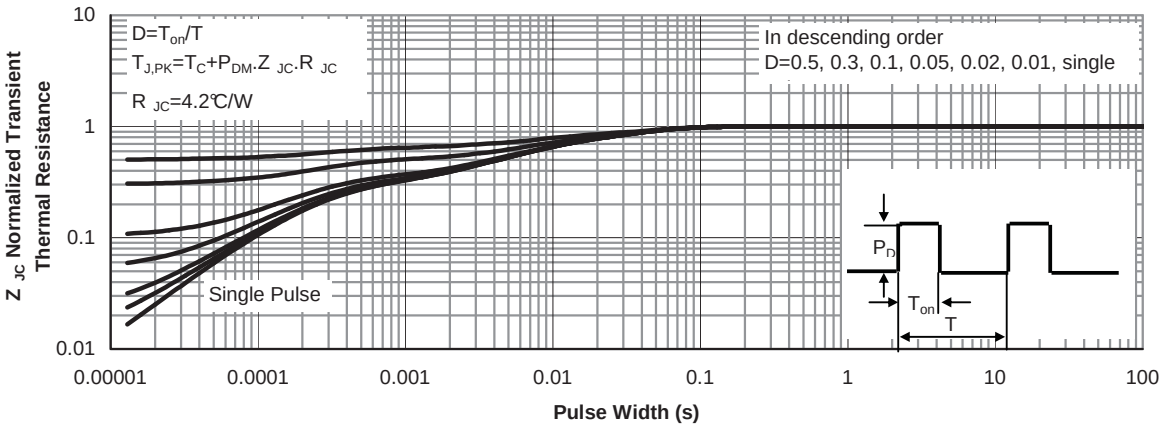


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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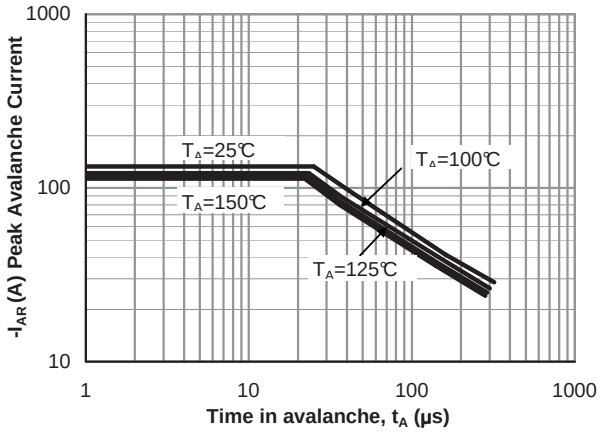


Figure 12: Single Pulse Avalanche capability (Note C)

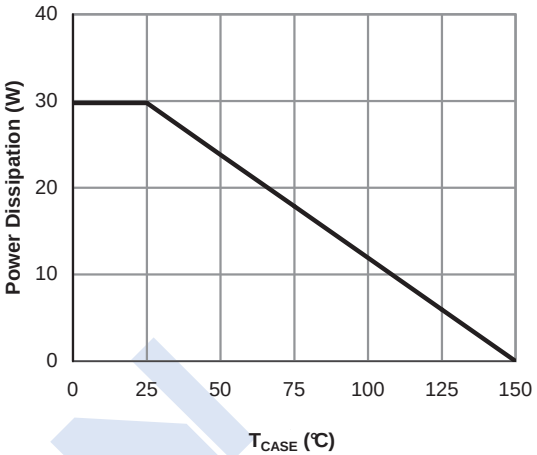


Figure 13: Power De-rating (Note F)

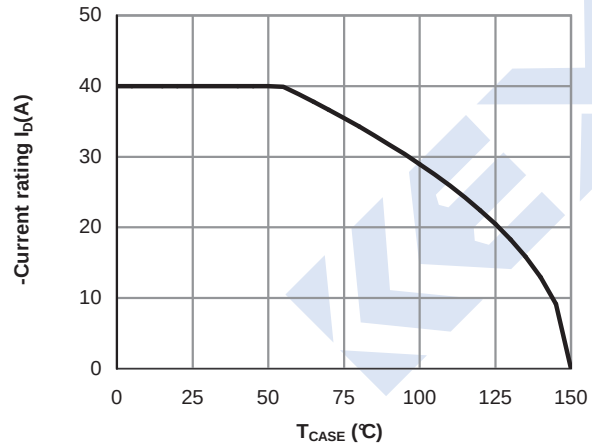


Figure 14: Current De-rating (Note F)

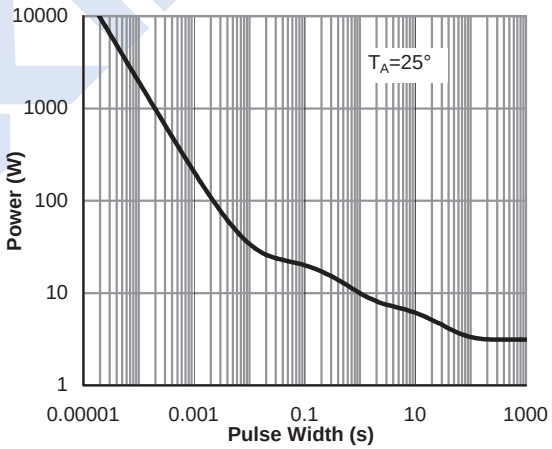


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

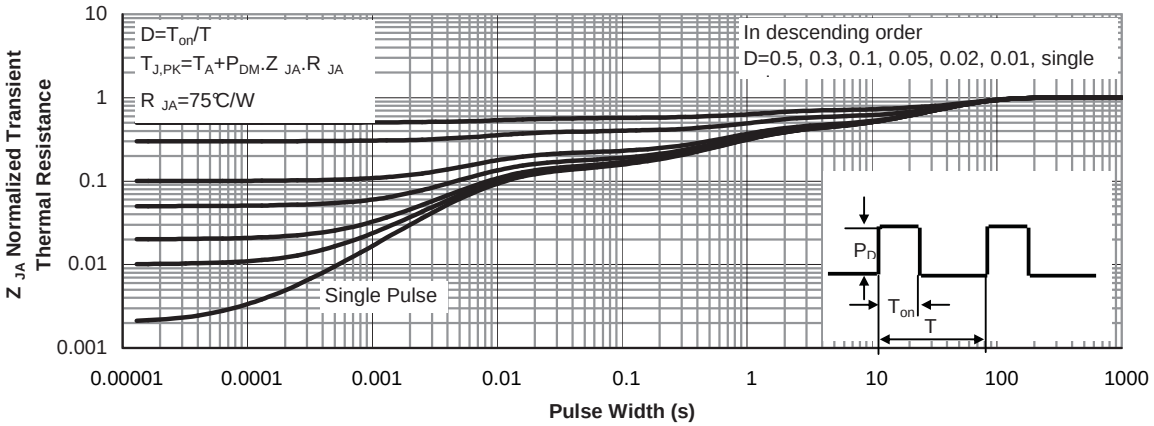


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

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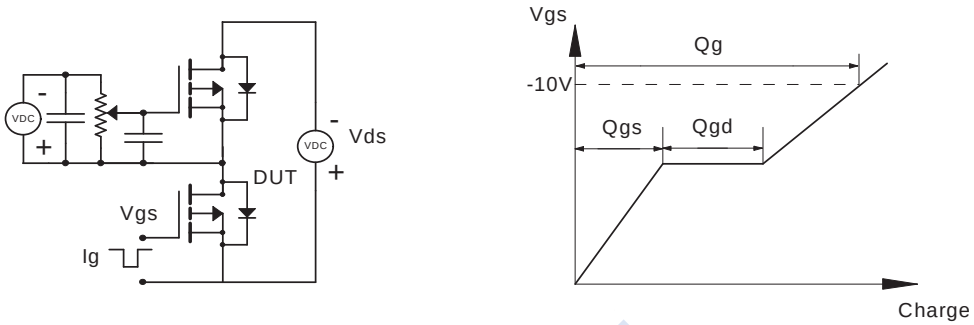
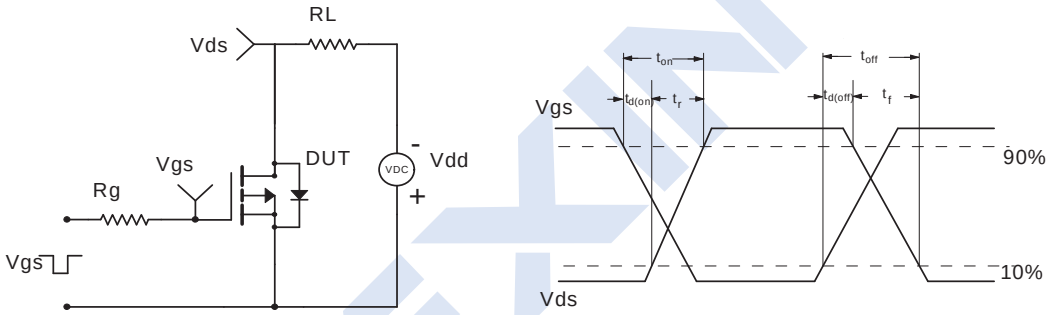
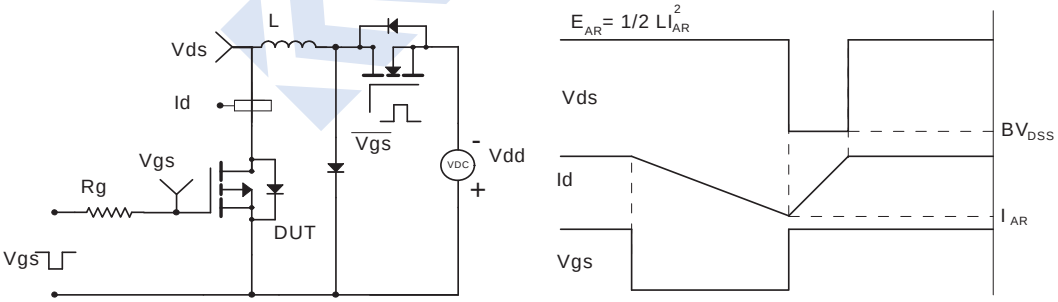
Gate Charge Test Circuit & Waveform



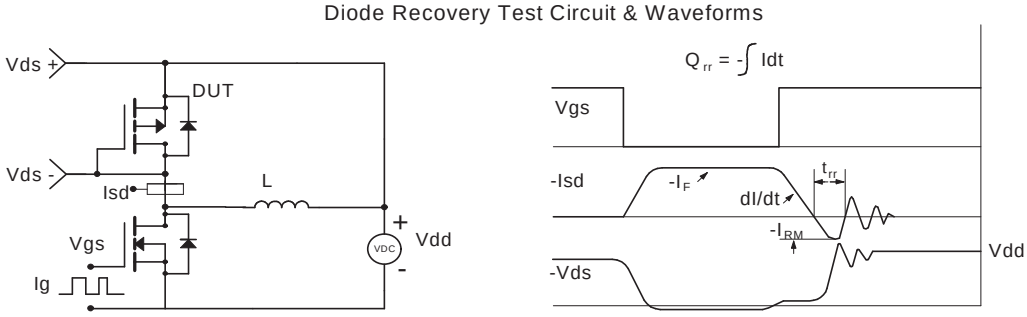

Resistive Switching Test Circuit & Waveforms




Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




Diode Recovery Test Circuit & Waveforms



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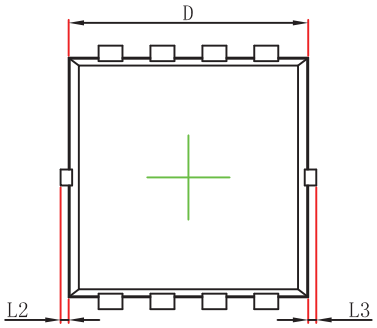
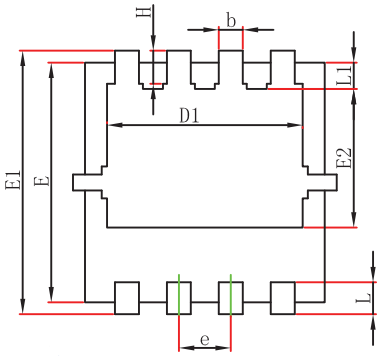
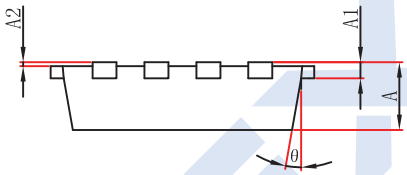
■ **PDFN3.3x3.3-8 Package Outline Dimensions**




Top View




Bottom View




Side View

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.650 | 0.850 | 0.026 | 0.033 |
| A1 | 0.152 REF. | | 0.006 REF. | |
| A2 | 0~0.05 | | 0~0.002 | |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D1 | 2.300 | 2.600 | 0.091 | 0.102 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 3.150 | 3.450 | 0.124 | 0.136 |
| E2 | 1.535 | 1.935 | 0.060 | 0.076 |
| b | 0.200 | 0.400 | 0.008 | 0.016 |
| e | 0.550 | 0.750 | 0.022 | 0.030 |
| L | 0.300 | 0.500 | 0.012 | 0.020 |
| L1 | 0.180 | 0.480 | 0.007 | 0.019 |
| L2 | 0~0.100 | | 0~0.004 | |
| L3 | 0~0.100 | | 0~0.004 | |
| H | 0.315 | 0.515 | 0.012 | 0.020 |
| θ | 9° | 13° | 9° | 13° |