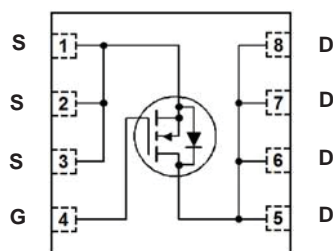


N-Channel MOSFET

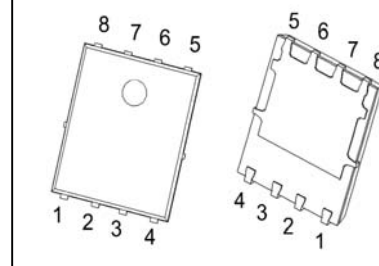
2KK6004DFN

■ Features

- V_{DS} (V) = 200 V
- $I_{D_{MAX}}$ (at $V_{GS} = 10$ V) = 20.2 A
- $R_{DS(ON)}$ (at $V_{GS} = 10$ V) < 50.5 m Ω
- $R_{DS(ON)}$ (at $V_{GS} = 7.5$ V) < 53.5 m Ω



DFN5x6-8(PDFNWB5x6-8L)

■ Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	200	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	20.2	A	
	$T_C = 70^\circ\text{C}$	16.1		
	$T_A = 25^\circ\text{C}$	6.2 ^{b, c}		
	$T_A = 70^\circ\text{C}$	5.0 ^{b, c}		
Pulsed Drain Current ($t = 100 \mu\text{s}$)	I_{DM}	50	A	
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	24		
	$T_A = 25^\circ\text{C}$	4.5 ^{b, c}		
Single Pulse Avalanche Current	$L = 0.1 \text{ mH}$	I_{AS}	20	
Single Pulse Avalanche Energy		E_{AS}	20	mJ
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	52	W
	$T_C = 70^\circ\text{C}$		33	
	$T_A = 25^\circ\text{C}$		5 ^{b, c}	
	$T_A = 70^\circ\text{C}$		3.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$	
Soldering Recommendations (Peak temperature) ^{d, e}		260		

■ Thermal resistance ratings

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	20	25	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	1.9	2.4	

Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- This is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 65 $^\circ\text{C/W}$.
- $T_C = 25^\circ\text{C}$.

N-Channel MOSFET

2KK6004DFN

■ Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\ \mu\text{A}$	-	165	-	mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	-6.8	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2	-	4	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 70^\circ\text{C}$	-	-	10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30	-	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	0.042	0.0505	Ω
		$V_{GS} = 7.5\text{ V}, I_D = 10\text{ A}$	-	0.043	0.0535	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$	-	35	-	S
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	1450	-	μF
Output Capacitance	C_{oss}		-	116	-	
Reverse Transfer Capacitance	C_{rss}		-	9.0	-	
Total Gate Charge	Q_g	$V_{DS} = 100\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	23.7	36	nC
		$V_{DS} = 100\text{ V}, V_{GS} = 7.5\text{ V}, I_D = 10\text{ A}$	-	18.3	28	
Gate-Source Charge	Q_{gs}	$V_{DS} = 100\text{ V}, V_{GS} = 7.5\text{ V}, I_D = 10\text{ A}$	-	6.3	-	nC
Gate-Drain Charge	Q_{gd}		-	6.0	-	
Output Charge	Q_{oss}		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	-	40.5	
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.2	1.0	1.8	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100\text{ V}, R_L = 10\ \Omega$ $I_D \leq 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	-	10	20	ns
Rise Time	t_r		-	18	36	
Turn-Off Delay Time	$t_{d(off)}$		-	17	34	
Fall Time	t_f		-	8	16	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100\text{ V}, R_L = 10\ \Omega$ $I_D \leq 10\text{ A}, V_{GEN} = 7.5\text{ V}, R_g = 1\ \Omega$	-	13	26	
Rise Time	t_r		-	29	58	
Turn-Off Delay Time	$t_{d(off)}$		-	16	32	
Fall Time	t_f		-	8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$	-	-	24	A
Pulse Diode Forward Current ($t = 100\ \mu\text{s}$)	I_{SM}		-	-	50	
Body Diode Voltage	V_{SD}	$I_S = 5\text{ A}$	-	0.81	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	-	165	330	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	570	1140	nC
Reverse Recovery Fall Time	t_b		-	70	-	ns
Reverse Recovery Rise Time	t_b		-	95	-	

Notes

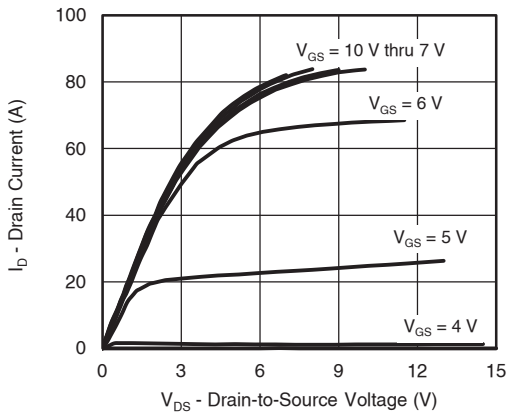
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

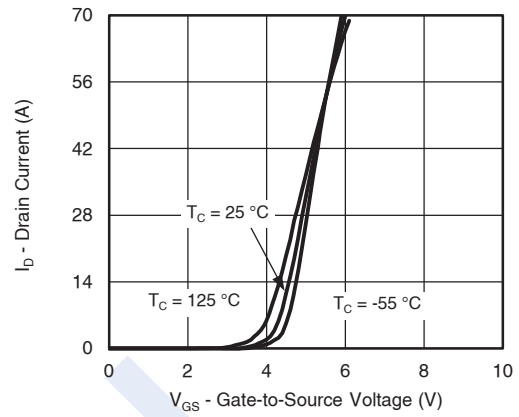
N-Channel MOSFET

2KK6004DFN

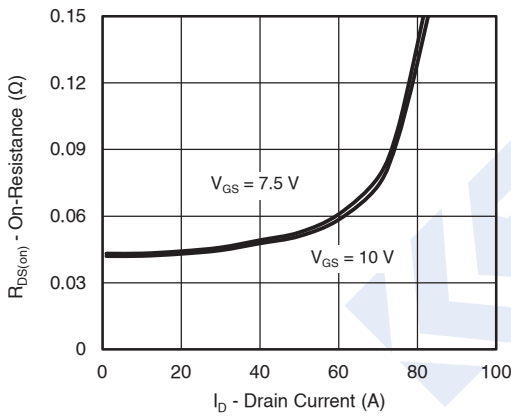
■ Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified



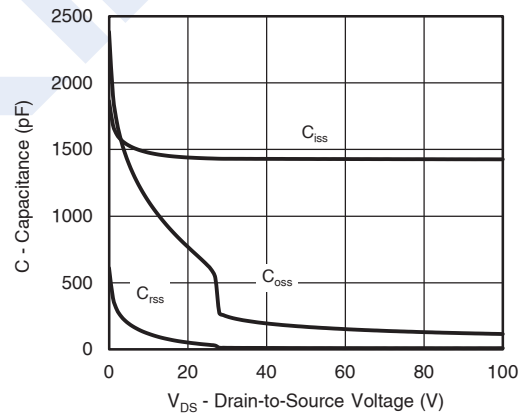
Output Characteristics



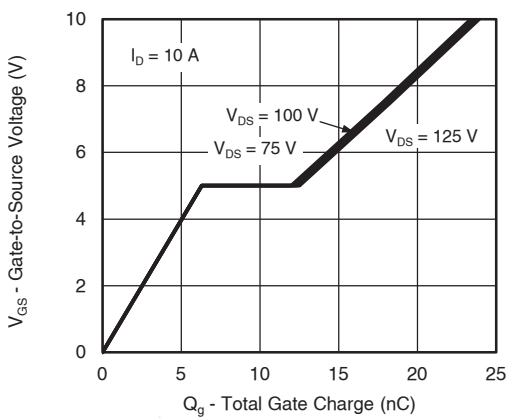
Transfer Characteristics



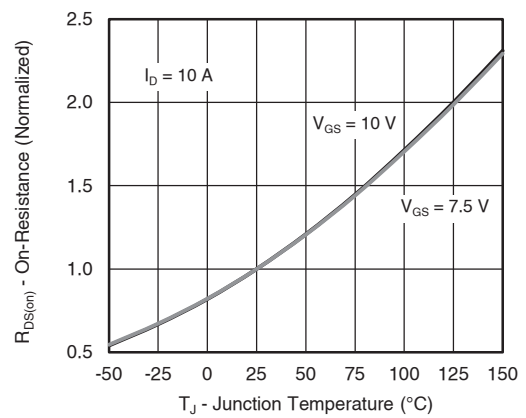
On-Resistance vs. Drain Current



Capacitance



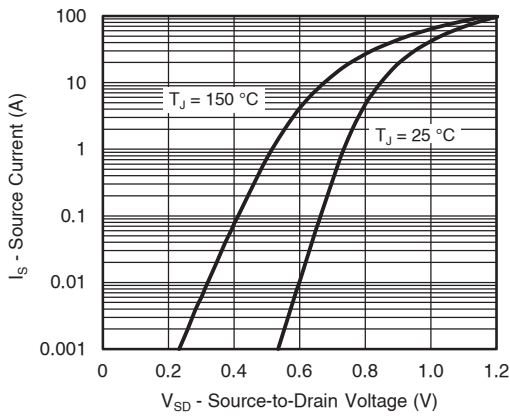
Gate Charge



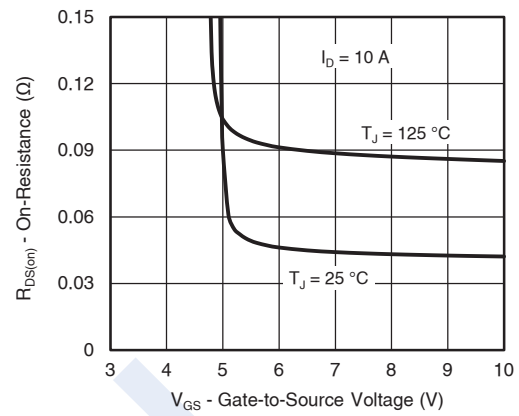
On-Resistance vs. Junction Temperature

N-Channel MOSFET

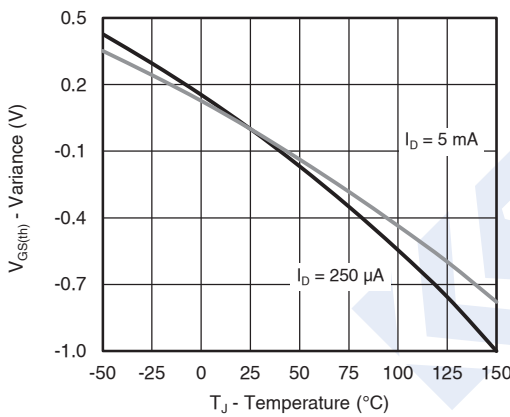
2KK6004DFN



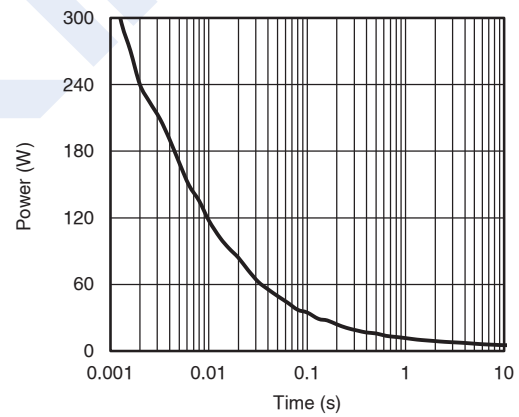
Source-Drain Diode Forward Voltage



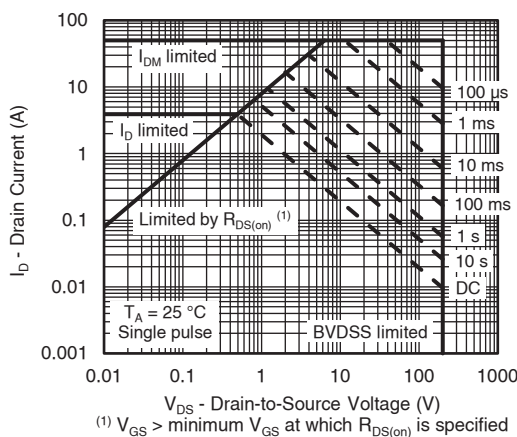
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



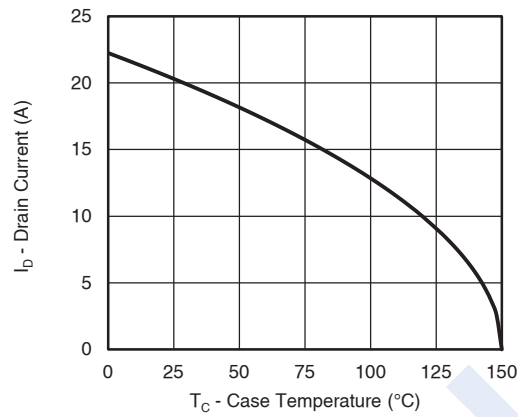
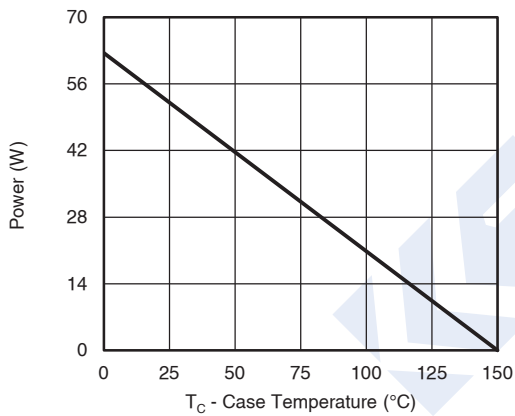
Single Pulse Power, Junction-to-Ambient



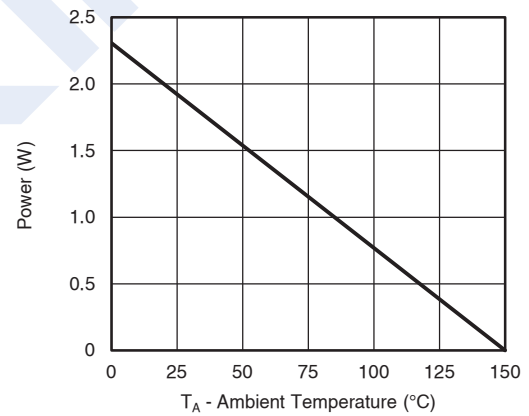
Safe Operating Area, Junction-to-Ambient

N-Channel MOSFET

2KK6004DFN

Current Derating ^a

Power, Junction-to-Case



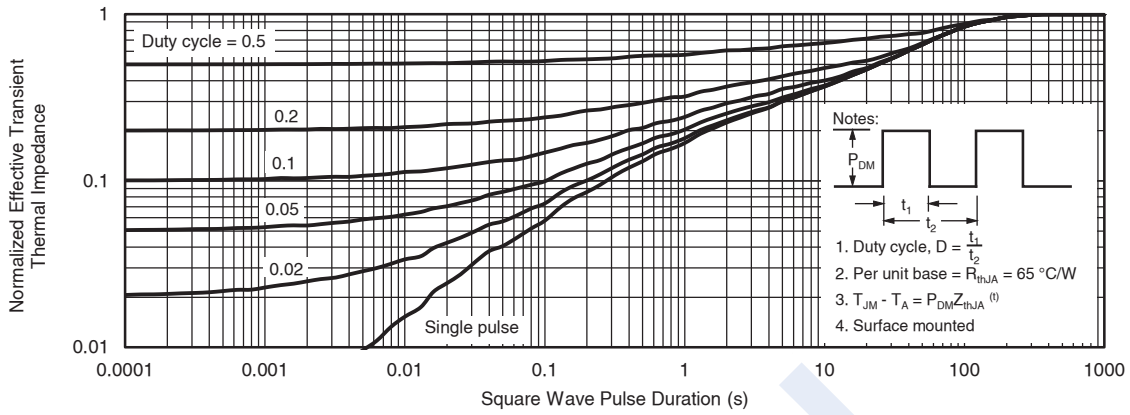
Power, Junction-to-Ambient

Note

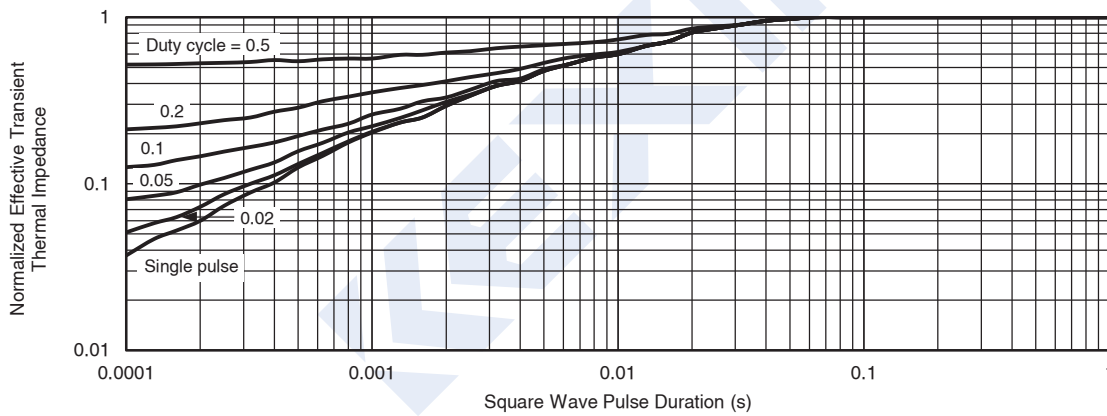
- a. The power dissipation P_D is based on T_J (max.) = 150 $^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-Channel MOSFET

2KK6004DFN



Normalized Thermal Transient Impedance, Junction-to-Ambient

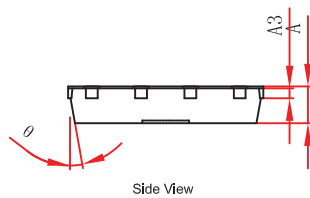
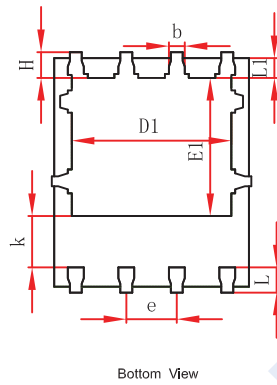
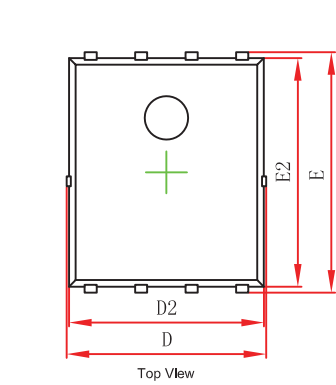


Normalized Thermal Transient Impedance, Junction-to-Case

N-Channel MOSFET

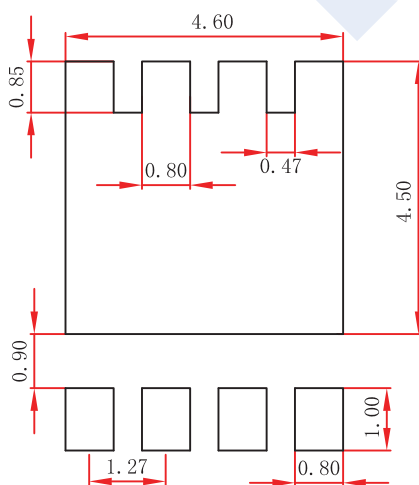
2KK6004DFN

DFN5x6-8(PDFNWB5x6-8L) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

DFN5x6-8(PDFNWB5x6-8L) Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.