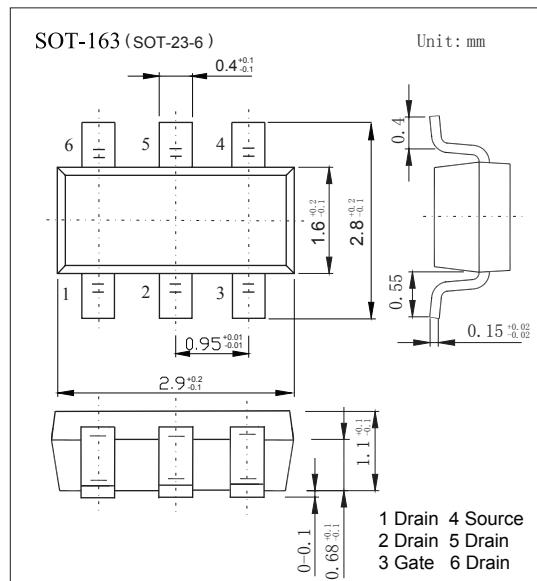
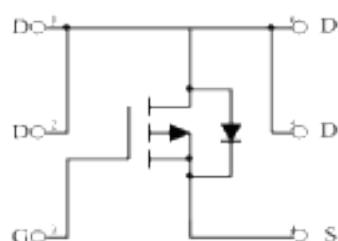


## P Channel MOSFET

### 2SJ3053DV

#### ■ Features

- Surface Mount Package
- Super High Density Cell Design  
for Extremely Low R<sub>D(on)</sub>
- Exceptional On-resistance and Maximum  
DC Current Capability



#### ■ Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-150	V
Gate-Source Voltage	V <sub>GSS</sub>	$\pm 20$	
Continuous Drain Current (Note 1)	I <sub>D</sub>	-1.4	A
Pulsed Drain Current ( $t_p=10\mu\text{s}$ )	I <sub>DM</sub>	-5	
Power Dissipation	P <sub>D</sub>	0.35	W
Thermal Resistance from Junction- to-Ambient (Note 1)	R <sub>thJA</sub>	357	°C/W
Junction Temperature	T <sub>J</sub>	150	°C
Junction Storage Temperature Range	T <sub>stg</sub>	-55 to 150	
Lead Temperature for Soldering Purposes(1/8" from case for 10 s)	T <sub>L</sub>	260	

Note 1.Surface mounted on FR4 board using the minimum recommended pad size.

## P Channel MOSFET

## 2SJ3053DV

■ Electrical Characteristics ( $T_a = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{DSS}$	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-150			V
Zero Gate Voltage Drain Current	$I_{DS(on)}$	$V_{DS} = -120\text{V}, V_{GS} = 0\text{V}$			-1	$\mu\text{A}$
Gate-Body Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$			$\pm 100$	nA
Gate Threshold Voltage (Note 2)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-2		-3	V
Static Drain-Source On-Resistance (Note 2)	$R_{DS(on)}$	$V_{GS} = -10\text{V}, I_D = -1.4\text{A}$			800	$\text{m}\Omega$
		$V_{GS} = -6\text{V}, I_D = -1\text{A}$			850	
Forward Transconductance (Note 2)	$g_{FS}$	$V_{DS} = -10\text{V}, I_D = -1.4\text{A}$		4.5		S
Diode Forward Voltage	$V_{SD}$	$I_S = -1\text{A}, V_{GS} = 0\text{V}$			-1.2	V
Dynamic Characteristics (Note 4)						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{V}, V_{DS} = -50\text{V}, f = 1\text{MHz}$		520		$\text{pF}$
Output Capacitance	$C_{oss}$			30		
Reverse Transfer Capacitance	$C_{rss}$			20		
Switching Characteristics (Note 3, 4)						
Total Gate Charge	$Q_g$	$V_{GS} = -6\text{V}, V_{DS} = -75\text{V}, I_D = -1\text{A}$		10	15	$\text{nC}$
Gate Source Charge	$Q_{gs}$			2.5		
Gate Drain Charge	$Q_{gd}$			5		
Turn-On Delay Time	$t_{d(on)}$	$V_{GEN} = -10\text{V}, V_{DD} = -75\text{V}, R_L = 75\Omega, I_D = -1\text{A}, R_G = 1\Omega$		10	20	$\text{ns}$
Turn-On Rise Time	$t_r$			12	25	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Turn-Off Fall Time	$t_f$			12	25	

Note 2. Pulse Test : Pulse width=300μs, duty cycle≤2%.

3. Switching characteristics are independent of operating junction temperature.

4. Garanted by design, not subject to producing.

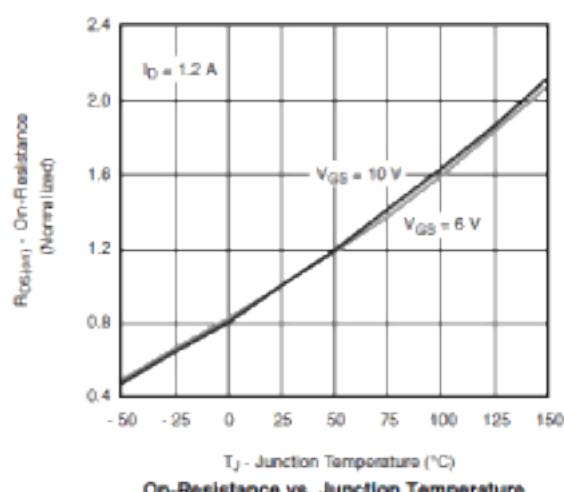
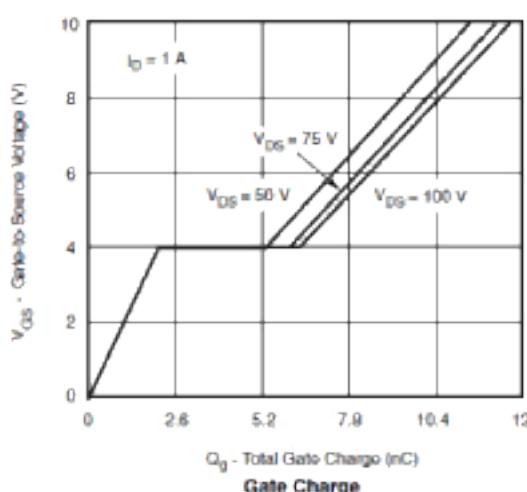
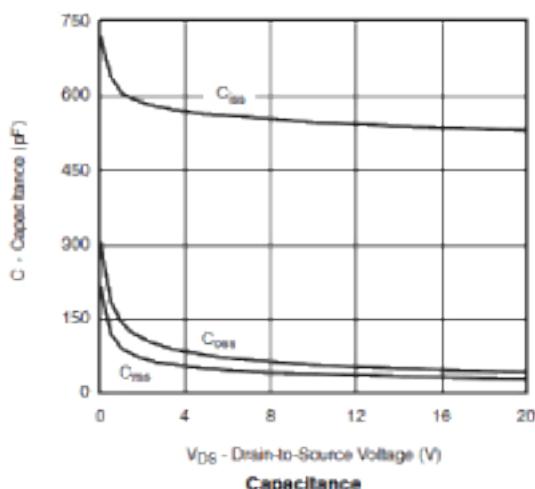
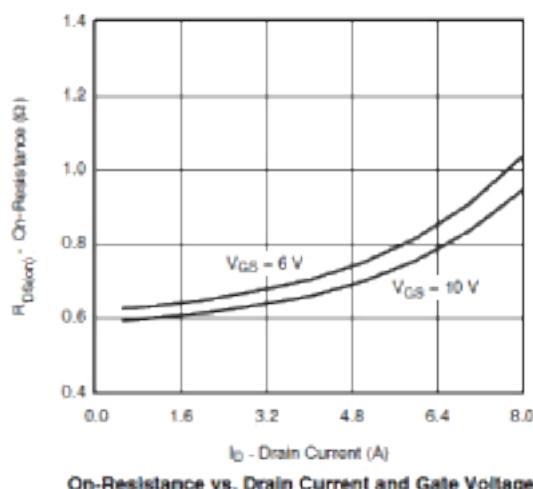
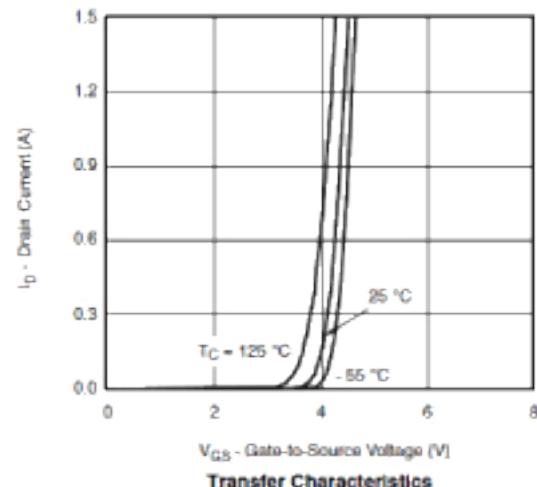
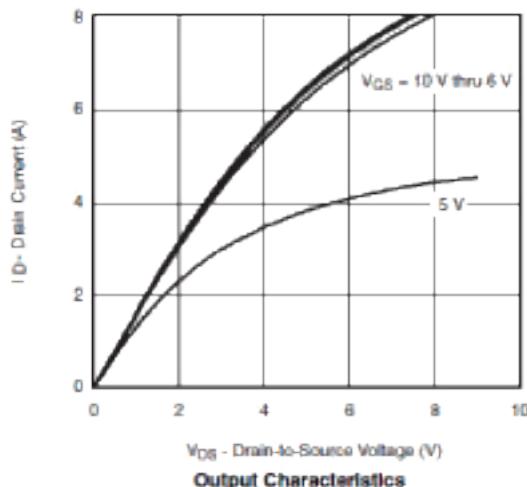
## ■ Marking

Marking	39W**
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## P Channel MOSFET

2SJ3053DV

## ■ Typical Characteristics



## P Channel MOSFET

## 2SJ3053DV

