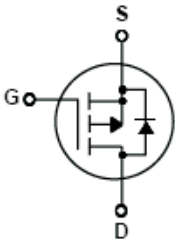
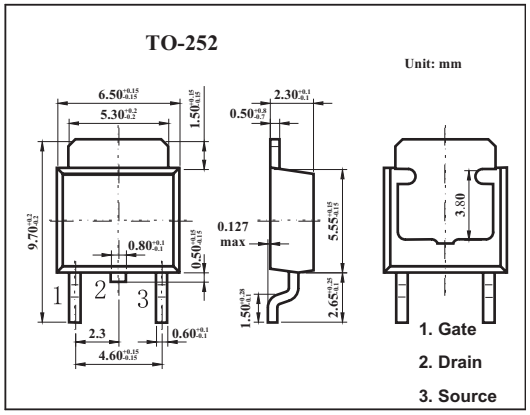
500V P-Channel MOSFET
KQD1P50

Features

- -1.2A, -500V, $R_{DS(on)}$ = 10.5Ω @V_{GS} = -10 V
- Low gate charge (typical 11 nC)
- Low Crss (typical 6.0 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability





Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	-500	V
Drain Current Continuous (Tc=25℃)	I_D	-1.2	A
Drain Current Continuous (Tc=100℃)		-0.76	A
Drain Current Pulsed *1	I_{DM}	-4.8	A
Gate-Source Voltage	V_{GSS}	±30	V
Single Pulsed Avalanche Energy*2	E_{AS}	110	mJ
Avalanche Current *1	I_{AR}	-1.2	A
Repetitive Avalanche Energy *1	E_{AR}	3.8	mJ
Peak Diode Recovery dv/dt *3	dv/dt	-4.5	V/ns
Power dissipation @ T_A=25℃	P_D	2.5	W
Power dissipation @ Tc=25℃	P_D	38	W
Derate above 25℃		0.3	W/℃
Operating and Storage Temperature	T_J, T_{STG}	-55 to150	℃
Maximum lead temperature for soldering purposes,1/8" from case for 5 seconds	T_L	300	℃
Thermal Resistance Junction to Case	$R_{\theta JC}$	3.29	℃/W
Thermal Resistance Junction to Ambient *4	$R_{\theta JA}$	50	℃/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	110	℃/W

*1 Repetitive Rating:Pulse width limited by maximum junction temperature

*2 l=138mH,I_{AS}=-1.2A,V_{DD}=-50V,R_G=25Ω,Startion T_J=25℃

*3 I_{SD}≤-1.5A,di/dt≤200A/μS,V_{DD}≤BV_{DSS},Startiong T_J=25℃

*4 When mounted on the minimum pad size recommended (PCB Mount)

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	B_{VDSS}	V_{GS} = 0 V, I_D = -250μA	-400			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = -250μA, Referenced to 25℃				mV/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -500 V, V_{GS} = 0 V			-1	μA
		V_{DS} = -400 V, T_C=125℃			-10	μA
Gate-Body Leakage Current,Forward	I_{GSSF}	V_{GS} = -30 V, V_{DS} = 0 V			-100	nA
Gate-Body Leakage Current,Reverse	I_{GSSR}	V_{GS} =30 V, V_{DS} = 0 V			100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-3.0		-5.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -0.6A		8.0	10.5	Ω
Forward Transconductance	g_{FS}	V_{DS} = -50 V, I_D =-0.6A *		1.12		S
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V,f = 1.0 MHz		270	230	pF
Output Capacitance	C_{oss}			40	50	pF
Reverse Transfer Capacitance	C_{rss}			6.0	8.0	pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -250 V, I_D = -1.5A,RG=25Ω *		9.0	30	ns
Turn-On Rise Time	tr			25	60	ns
Turn-Off Delay Time	$t_{d(off)}$			27	65	ns
Turn-Off Fall Time	t_f			30	70	ns
Total Gate Charge	Q_g	V_{DS} = -400 V, I_D = -1.5A,V_{GS} = -10 V *		11	14	nC
Gate-Source Charge	Q_{gs}			2.0		nC
Gate-Drain Charge	Q_{gd}			5.6		nC
Maximum Continuous Drain-Source Diode Forwrad Current	I_S				-1.2	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				-4.8	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S =-1.2 A			-5.0	V
Diode Reverse Recovery Time	t_{rr}	V_{GS} = 0 V,dI_F/dt = 100 A/μs,I_S=-1.5A*		200		ns
Diode Reverse Recovery Current	Q_{rr}			0.7		μC

* Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%