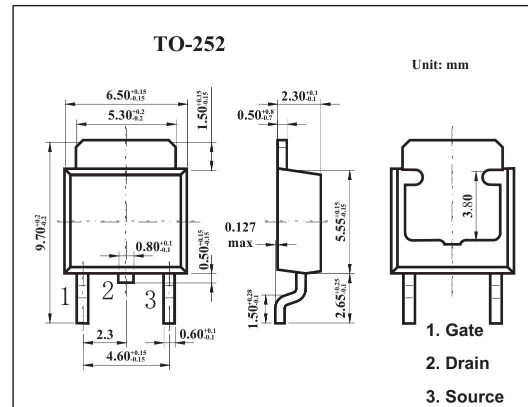
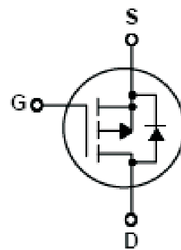
500V P-Channel MOSFET
KQD3P50



Features

- -1.2A, -500V, $R_{DS(on)}$ = 4.9Ω @V_{GS} = -10 V
- Low gate charge (typical 18 nC)
- Low Crss (typical9.5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	-500	V
Drain Current Continuous (Tc=25℃)	I_D	-2.1	A
Drain Current Continuous (Tc=100℃)		-1.33	A
Drain Current Pulsed *1	I_{DM}	-8.4	A
Gate-Source Voltage	V_{GSS}	±30	V
Single Pulsed Avalanche Energy*2	E_{AS}	250	mJ
Avalanche Current *1	I_{AR}	-2.1	A
Repetitive Avalanche Energy *1	E_{AR}	5	mJ
Peak Diode Recovery dv/dt *3	dv/dt	-4.5	V/ns
Power dissipation @ TA=25℃	P_D	2.5	W
Power dissipation @ Tc=25℃	P_D	50	W
Derate above 25℃		0.4	W/℃
Operating and Storage Temperature	T_J, T_{STG}	-55 to150	℃
Maximum lead temperature for soldering purposes,1/8" from case for 5 seconds	T_L	300	℃
Thermal Resistance Junction to Case	$R_{\theta JC}$	2.5	℃/W
Thermal Resistance Junction to Ambient *4	$R_{\theta JA}$	50	℃/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	110	℃/W

*1 Repetitive Rating:Pulse width limited by maximum junction temperature

*2 l=102mH,I_{AS}=-2.1A,V_{DD}=-50V,R_G=25Ω,Startion T_J=25℃

*3 I_{SD}≤-2.7A,di/dt≤200A/μS,V_{DD}≤B_{VDSS},Startiong T_J=25℃

*4 When mounted on the minimum pad size recommended (PCB Mount)

KQD3P50

■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = -250 μ A	-500			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = -250 μ A, Referenced to 25℃		0.42		mV/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -500 V, V_{GS} = 0 V			-1	μ A
		V_{DS} = -400 V, T_C=125℃			-10	μ A
Gate-Body Leakage Current,Forward	I_{GSSF}	V_{GS} = -30 V, V_{DS} = 0 V			-100	nA
Gate-Body Leakage Current,Reverse	I_{GSSR}	V_{GS} =30 V, V_{DS} = 0 V			100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 μ A	-3.0		-5.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -1.05A		3.9	4.9	Ω
Forward Transconductance	g_{FS}	V_{DS} = -50 V, I_D =-1.05A *		2.1		S
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V,f = 1.0 MHz		510	660	pF
Output Capacitance	C_{oss}			70	90	pF
Reverse Transfer Capacitance	C_{rss}			9.5	12	pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -250 V, I_D = -2.7A,RG=25 Ω *		12	35	ns
Turn-On Rise Time	t_r			56	120	ns
Turn-Off Delay Time	$t_{d(off)}$			35	80	ns
Turn-Off Fall Time	t_f			45	100	ns
Total Gate Charge	Q_g	V_{DS} = -400 V, I_D = -2.7A,V_{GS} = -10 V *		18	23	nC
Gate-Source Charge	Q_{gs}			3.6		nC
Gate-Drain Charge	Q_{gd}			9.2		nC
Maximum Continuous Drain-Source Diode Forwrad Current	I_S				-2.1	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				-8.4	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S =-2.1 A			-5.0	V
Diode Reverse Recovery Time	t_{rr}	V_{GS} = 0 V,dI_F/d_t = 100 A/ μ s,I_S=-2.7A*		200		ns
Diode Reverse Recovery Current	Q_{rr}			1.5		μ C

* Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle ≤ 2.0%