# TVS Diode Array

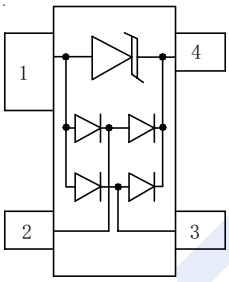
# SR05

## ■ Features

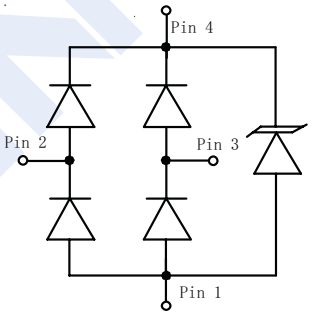
- ESD protection to
  **IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)**
  **IEC 61000-4-4 (EFT) 40A (5/50ns)**
  **IEC 61000-4-5 (Lightning) 24A (8/20μs)**
- Array of surge rated diodes with internal TVS Diode
- Protects two I/O lines
- Low capacitance (<10pF) for high-speed interfaces
- Low clamping voltage
- Low operating voltage: 5.0V
- Solid-state silicon-avalanche technology
- Marking : R05

## ■ Applications

- USB Power & Data Line Protection
- Ethernet 10BaseT
- $I^2C$ Bus Protection
- Video Line Protection
- T1/E1 secondary IC Side Protection
- Portable Electronics
- Microcontroller Input Protection
- WAN/LAN Equipment
- ISDN S/T Interface



PIN Configuration



Circuit Diagram

## ■ Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Peak pulse power (tp = 8/20μs) | $P_{pk}$ | 500 | W |
| Peak pulse current (tp = 8/20μs) | $I_{PP}$ | 25 | A |
| Peak forward voltage ($I_F$ = 1A, tp = 8/20μs) | $V_{FP}$ | 1.5 | V |
| Lead soldering temperature | $T_L$ | 260 (10 sec.) | ℃ |
| Operating temperature | $T_J$ | -55 to +125 | |
| Storage temperature | $T_{stg}$ | -55 to +150 | |

## ■ Electrical Characteristics

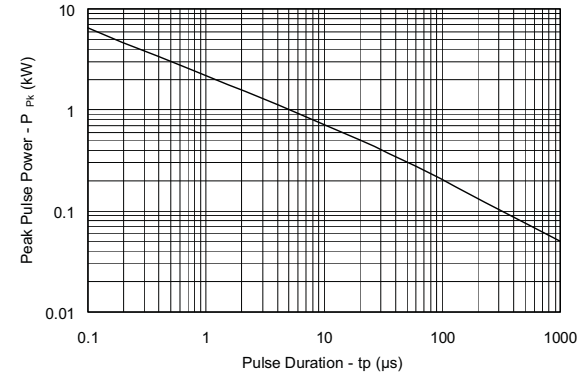
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Reverse stand-off voltage | $V_{RWM}$ | | | | 5 | V |
| Reverse breakdown voltage | $V_{BR}$ | It= 1mA | 6 | | | |
| Reverse leakage current | $I_R$ | $V_{RWM}$ = 5 V, T = 25℃ | | | 5 | μA |
| Clamping voltage (tp=8/20μs) | $V_C$ | $I_{PP}$=1A | | | 9.8 | V |
| Clamping voltage (tp=8/20μs) | $V_C$ | $I_{PP}$=10A | | | 12 | |
| Clamping voltage (tp=8/20μs) | $V_C$ | $I_{PP}$=25A | | | 20 | |
| Junction capacitance | $C_J$ | $V_R$ = 0Vdc, f=1MHz Between I/O pins and GND | | 6 | 10 | pF |
| | | $V_R$ = 0Vdc, f=1MHz Between I/O pins | | 3 | | |

# TVS Diode Array

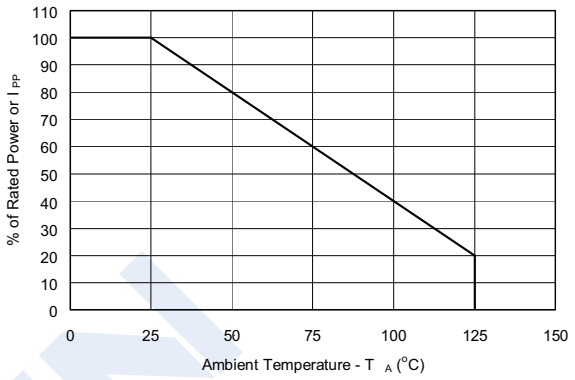
## SR05

■ Typical Characteristics

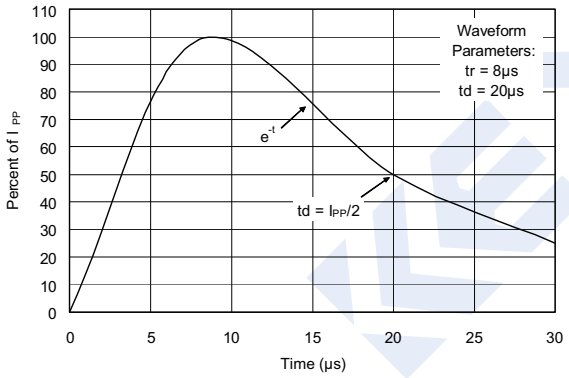
Non-Repetitive Peak Pulse Power vs. Pulse Time



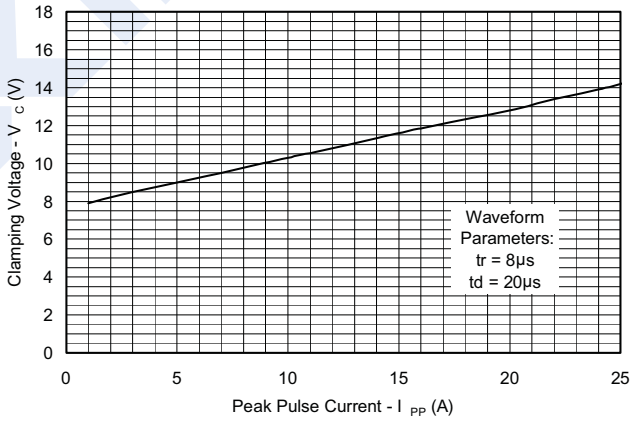

Power Derating Curve



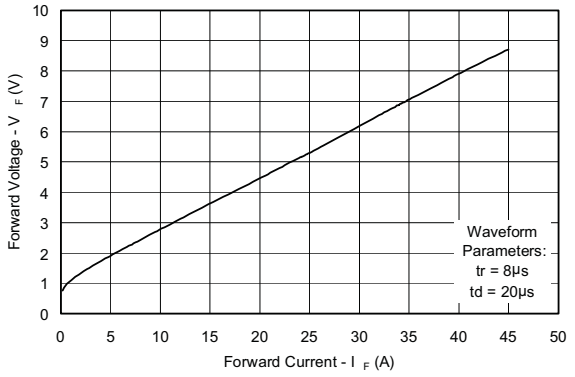

Pulse Waveform



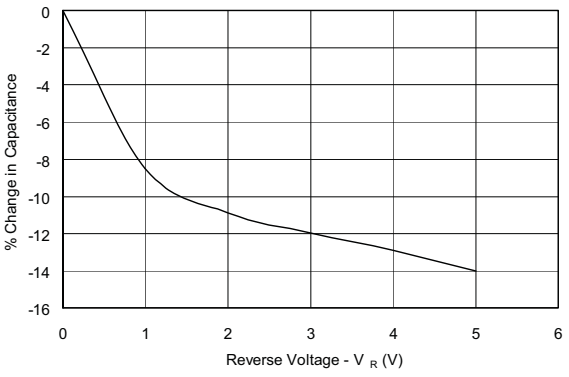

Clamping Voltage vs. Peak Pulse Current




Forward Voltage vs. Forward Current




Capacitance vs. Reverse Voltage



# TVS Diode Array

## SR05

■ Applications Information

### Device Connection Options for Protection of Two High-Speed Data Lines

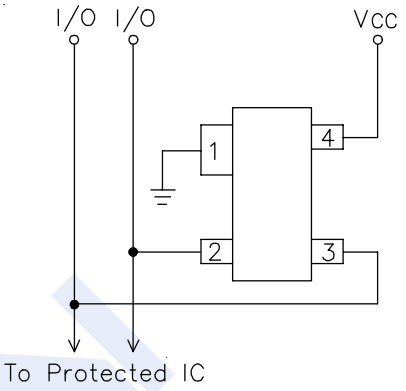
The SR05 TVS is designed to protect two data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode $V_F$) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 2 and 3. The negative reference (REF1) is connected at pin 1. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance.
The positive reference (REF2) is connected at pin 4. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 4 directly to the positive supply rail ($V_{CC}$). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. The SR05 can be isolated from the power supply by adding a series resistor between pin 4 and $V_{CC}$. A value of 10k is recommended. The internal TVS and steering diodes remain biased, providing the advantage of lower capacitance.
3. In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pin 4 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

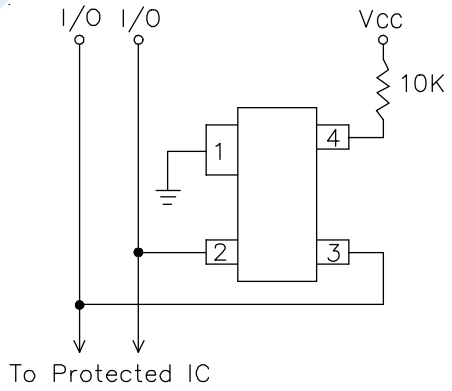
### ESD Protection With SR05

SR05 are optimized for ESD protection using the rail-to-rail topology. Along with good board layout, these devices virtually eliminate the disadvantages of using discrete components to implement this topology. Consider the situation shown in Figure 1 where discrete diodes or diode arrays are configured for rail-to-rail protection on a high speed line. During positive duration ESD events, the top diode will be forward biased when the voltage on the protected line exceeds the reference voltage plus the $V_F$ drop of the diode.

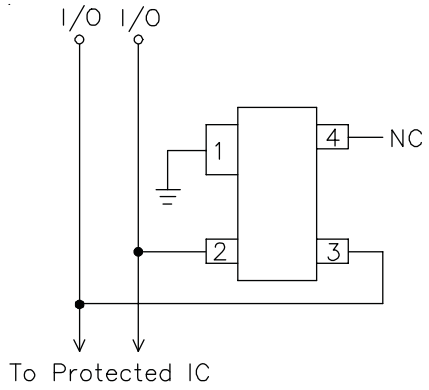
### Data Line and Power Supply Protection Using Vcc as reference




### Data Line Protection with Bias and Power Supply Isolation Resistor




### Data Line Protection Using Internal TVS Diode as Reference



# TVS Diode Array

## SR05

■ Applications Information (continued)

For negative events, the bottom diode will be biased when the voltage exceeds the $V_F$ of the diode. At first approximation, the clamping voltage due to the characteristics of the protection diodes is given by:

$V_C = V_{CC} + V_F$ (for positive duration pulses)
$V_C = -V_F$ (for negative duration pulses)

However, for fast rise time transient events, the effects of parasitic inductance must also be considered as shown in Figure 2. Therefore, the actual clamping voltage seen by the protected circuit will be:

$V_C = V_{CC} + V_F + L_P di_{ESD}/dt$ (for positive duration pulses)
$V_C = -V_F - L_G di_{ESD}/dt$ (for negative duration pulses)

ESD current reaches a peak amplitude of 30A in 1ns for a level 4 ESD contact discharge per IEC 61000-4-2. Therefore, the voltage overshoot due to 1nH of series inductance is:

$V = L_P di_{ESD}/dt = 1X10^{-9} (30 / 1X10^{-9}) = 30V$

Example:
Consider a $V_{CC}$ = 5V, a typical $V_F$ of 30V (at 30A) for the steering diode and a series trace inductance of 10nH. The clamping voltage seen by the protected IC for a positive 8kV (30A) ESD pulse will be:

$V_C$ = 5V + 30V + (10nH X 30V/nH) = 335V

This does not take into account that the ESD current is directed into the supply rail, potentially damaging any components that are attached to that rail. Also note that it is not uncommon for the $V_F$ of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. It is also possible that the power dissipation capability of the discrete diode will be exceeded, thus destroying the device.

The SR05 is designed to overcome the inherent disadvantages of using discrete signal diodes for ESD suppression. The SR05's integrated TVS diode helps to mitigate the effects of parasitic inductance in

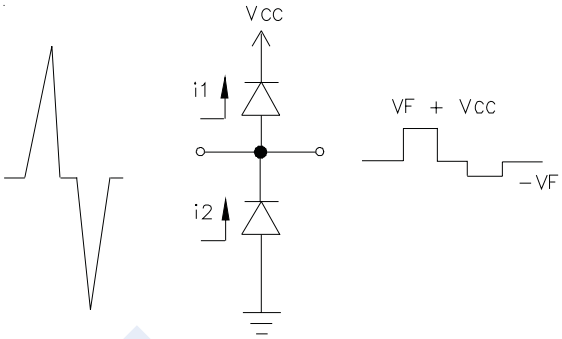



**Figure 1 - "Rail-To-Rail" Protection Topology (First Approximation)**

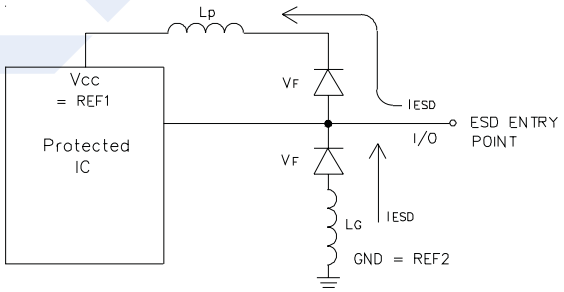



**Figure 2 - The Effects of Parasitic Inductance When Using Discrete Components to Implement Rail-To-Rail Protection**

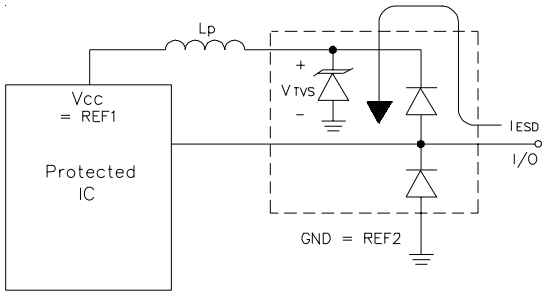



**Figure 3 - Rail-To-Rail Protection Using TVS Arrays**

# TVS Diode Array

## SR05

■ Applications Information (continued)

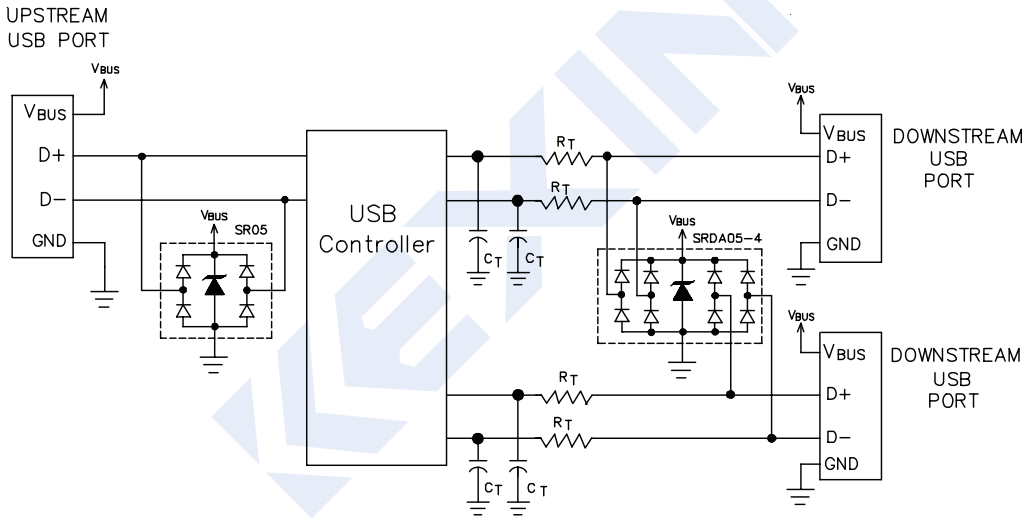
the power supply connection. During an ESD event, the current will be directed through the integrated TVS diode to ground. The total clamping voltage seen by the protected IC due to this path will be:

$V_C = V_{F(Clamp)} + V_{TVS}$

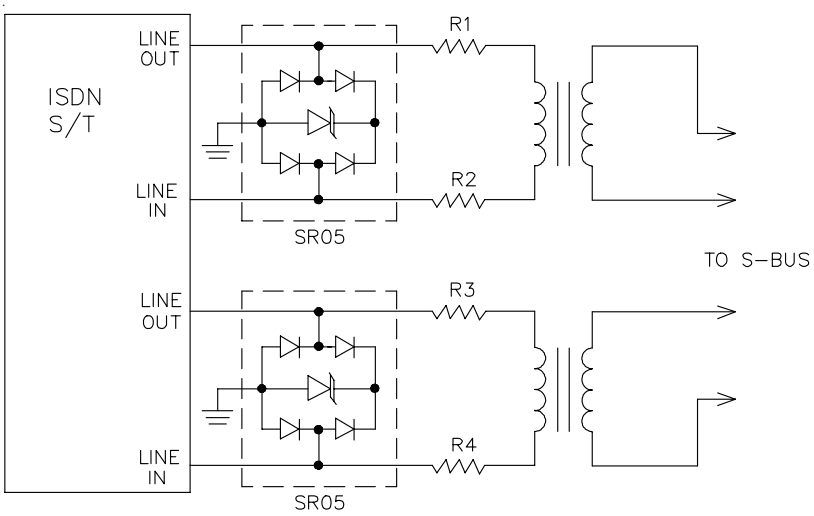
This is given in the data sheet as the rated clamping voltage of the device. For a SR05 the typical clamping voltage is <16V at $I_{PP}$=30A. The diodes internal to the SR05 are low capacitance, fast switching devices that are rated to handle transient currents and maintain excellent forward voltage characteristics.

Universal Serial Bus ESD Protection

The figure below illustrates how to use the SR05 to protect one upstream USB port and the SRDA05-4 to protect two downstream USB ports. When the voltage on the data lines exceed the bus voltage (plus one diode drop), the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The TVS diode directs the surge to ground. The TVS diode also acts to suppress ESD strikes directly on the voltage bus. Thus, both power and data pins are protected with a single device.




Universal Serial Bus ESD Protection



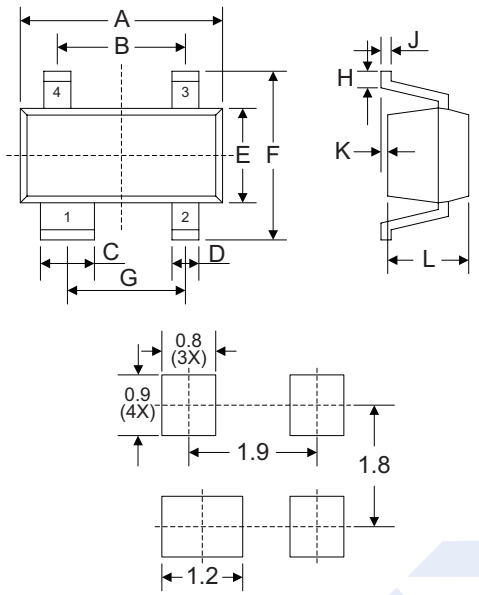

ISDN S/T Interface Protection

# TVS Diode Array

## SR05

■ Package Outline Dimensions

SOT-143




Recommended Soldering Pad Layout

| Symbol | Dimension | | | |
|---|---|---|---|---|
| | Millimeters | | Inches | |
| | Min. | Max. | Min. | Max. |
| A | 2.79 | 3.04 | 0.110 | 0.120 |
| B | 1.90 | | 0.075 | |
| C | 0.76 | 0.93 | 0.030 | 0.037 |
| D | 0.36 | 0.50 | 0.014 | 0.020 |
| E | 1.19 | 1.40 | 0.047 | 0.055 |
| F | - | 2.50 | - | 0.098 |
| G | 1.70 | | 0.067 | |
| H | 0.15 | - | 0.006 | - |
| J | 0.08 | 0.15 | 0.003 | 0.006 |
| K | - | 0.13 | - | 0.005 |
| L | - | 1.14 | - | 0.045 |